

Lead Free Package and Finish

N-channel 650V, 7A Power MOSFET

Description

The Power MOSFET is fabricated using the advanced planar VDMOS technology. The resulting device has low conduction resistance, superior switching performance and high avalanche energy.

Features

- ◆ Low $R_{DS(on)}$
- ◆ Low gate charge (typ. $Q_g = 20.7\text{nC}$)
- ◆ 100% UIS tested
- ◆ RoHS compliant

Applications

- ◆ Power factor correction.
- ◆ Switched mode power supplies.
- ◆ LED driver.

Product Summary

V_{DSS}	650V
I_D	7A
$R_{DS(on),max}$	1.4Ω
$Q_{g,typ}$	20.7nC



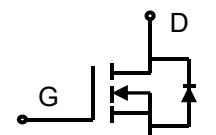
TO-220F



TO-220



TO-252



N-Channel MOSFET



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	650	V
Continuous drain current ($T_c = 25^\circ\text{C}$) ($T_c = 100^\circ\text{C}$)	I_D	7 4.3	A A
Pulsed drain current ¹⁾	I_{DM}	28	A
Gate-Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse ²⁾	E_{AS}	352	mJ
Peak diode recovery dv/dt ³⁾	dv/dt	5	V/ns
Power Dissipation TO-220F ($T_c = 25^\circ\text{C}$) Derate above 25°C	P_D	39 0.31	W W/ $^\circ\text{C}$
Power Dissipation TO-220\ TO-252 ($T_c = 25^\circ\text{C}$) Derate above 25°C		100 0.8	W W/ $^\circ\text{C}$
Operating junction and storage temperature range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Continuous diode forward current	I_S	7	A
Diode pulse current	$I_{S,pulse}$	28	A

Thermal Characteristics

Parameter	Symbol	Value		Unit
		TO-220F	TO-220\TO-252	
Thermal resistance, Junction-to-case	$R_{\theta JC}$	3.2	1.25	$^\circ\text{C/W}$
Thermal resistance, Junction-to-ambient	$R_{\theta JA}$	62.5	110	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device	Device Package	Marking	Units/Tube	Units/Real
JMA7N65C	TO-220	JMA7N65C	50	
RT F7N65Ô	TO-220F	RT ÔÍ þÍ Ó	50	
RT Ó7N65Ô	TO-252	RT ÓÍ þÍ Ó		2500

Electrical Characteristics

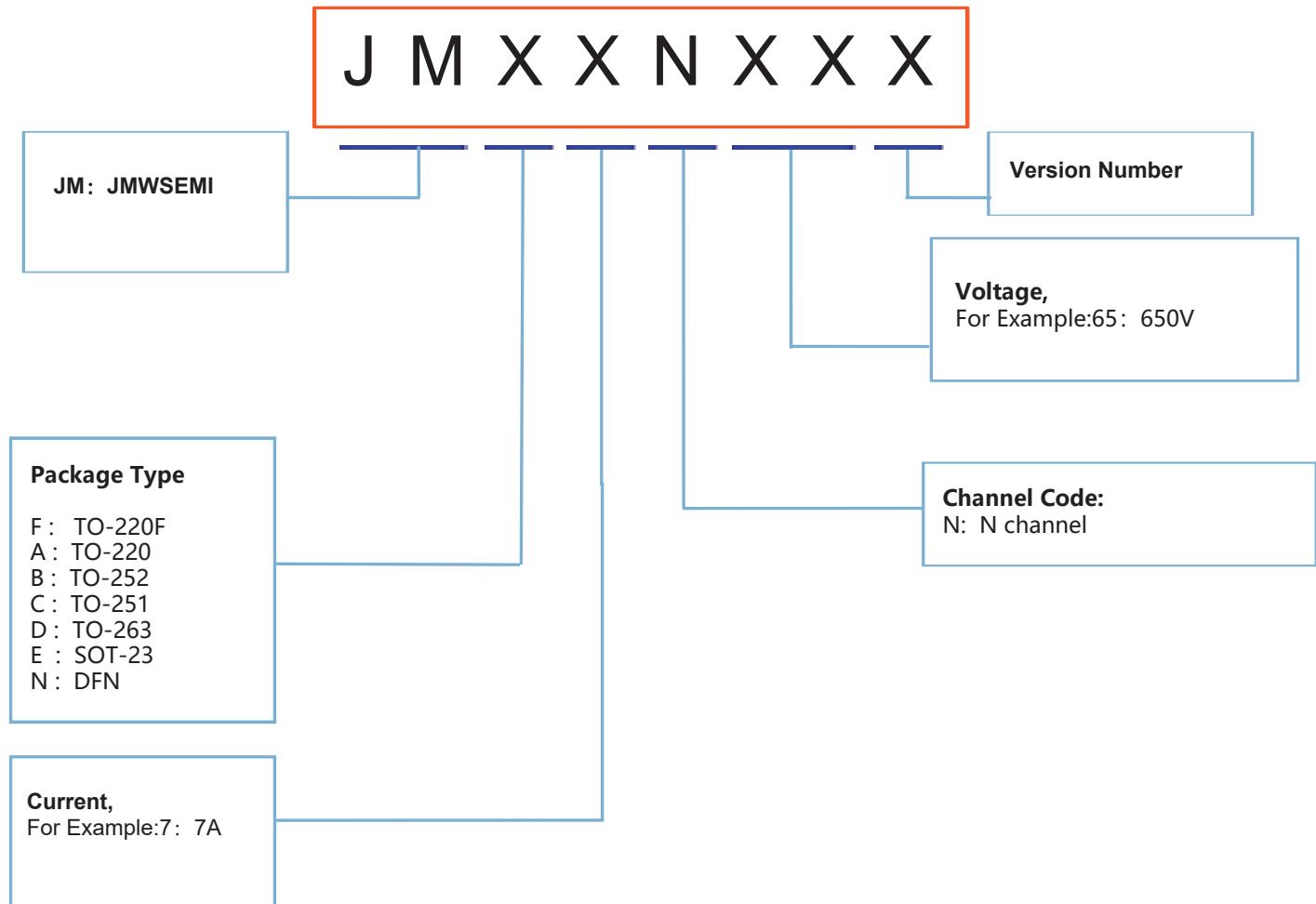
T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250 uA	650	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250 uA	2	-	4	V
Drain cut-off current	I _{DSS}	V _{DS} =650 V, V _{GS} =0 V, T _j = 25°C T _j = 125°C	-	-	1 100	µA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =30 V, V _{DS} =0 V	-	-	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-30 V, V _{DS} =0 V	-	-	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =3.5 A	-	1.2	1.4	Ω
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	1090	-	pF
Output capacitance	C _{oss}		-	111	-	
Reverse transfer capacitance	C _{rss}		-	6.1	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 325 V, I _D = 7 A R _G = 10 Ω, V _{GS} =15 V	-	12.2	-	ns
Rise time	t _r		-	33.4	-	
Turn-off delay time	t _{d(off)}		-	53.6	-	
Fall time	t _f		-	15	-	
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DD} =520 V, I _D =7 A, V _{GS} =0 to 10 V	-	5.7	-	nC
Gate to drain charge	Q _{gd}		-	7.2	-	
Gate charge total	Q _g		-	20.7	-	
Gate plateau voltage	V _{plateau}		-	5	-	
Reverse diode characteristics						
Diode forward voltage	V _{SD}	V _{GS} =0 V, I _F =7 A	-	0.85	1.5	V
Reverse recovery time	t _{rr}	V _R =325 V, I _F =7 A, dI _F /dt=100 A/µs	-	373.2	-	ns
Reverse recovery charge	Q _{rr}		-	2.1	-	
Peak reverse recovery current	I _{rrm}		-	15.7	-	

Notes:

1. Pulse width limited by maximum junction temperature.
2. L=10mH, I_{AS} = 8.4A, Starting T_j = 25°C.
3. I_{SD} = 7A, dI/dt≤100A/us, V_{DD}≤BV_{DS}, Starting T_j = 25°C.

VD MOS Product Names Rules



Electrical Characteristics Diagrams

Figure 1. Typical Output Characteristics

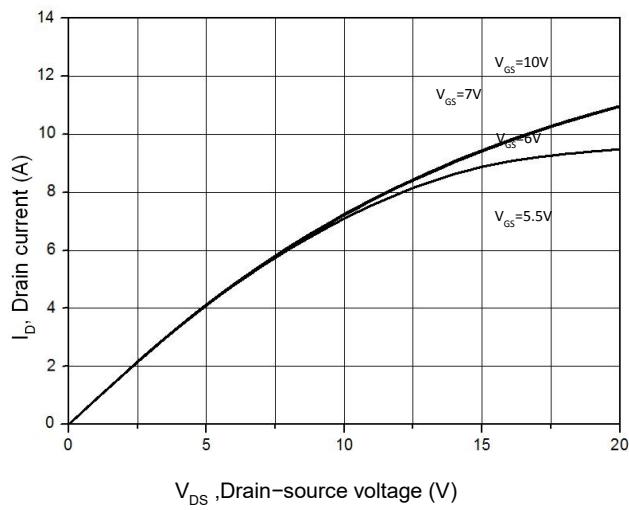


Figure 2. Transfer Characteristics

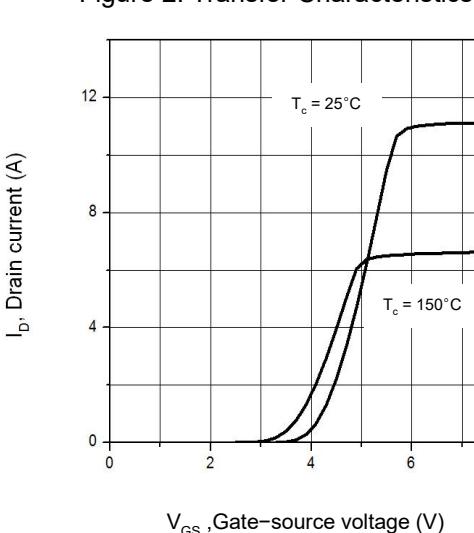


Figure 3. On-Resistance Variation vs. Drain Current

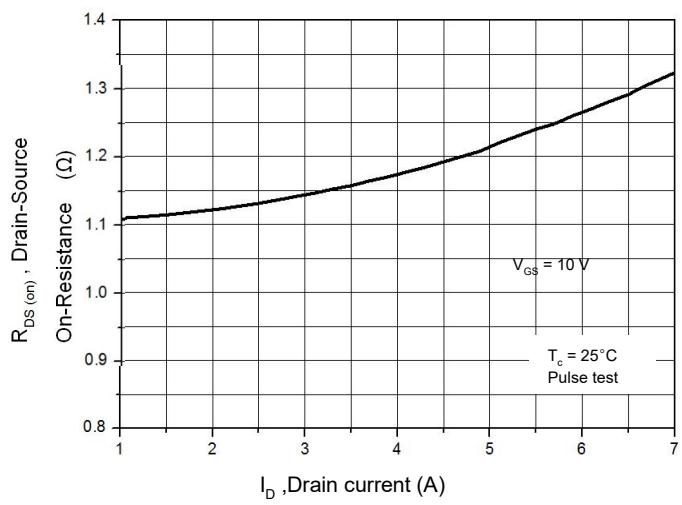


Figure 4. Threshold Voltage vs. Temperature

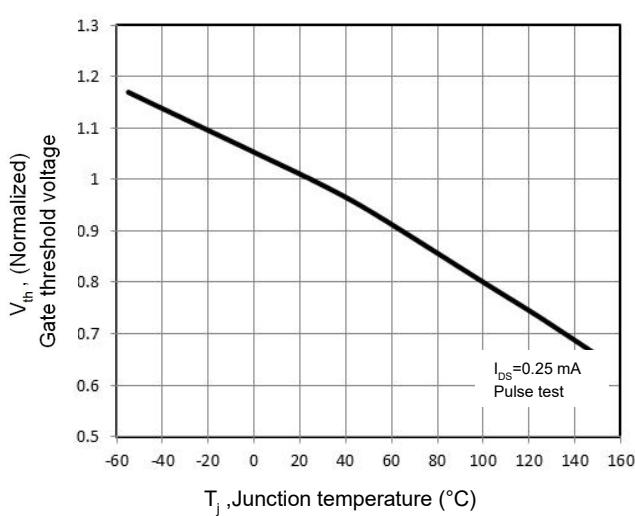


Figure 5. Breakdown Voltage vs. Temperature

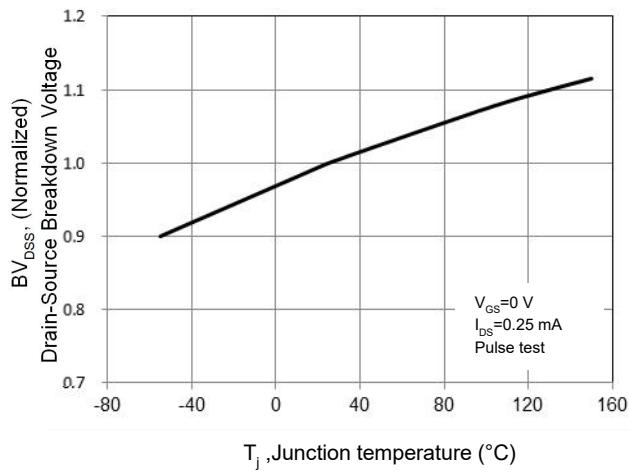


Figure 6. On-Resistance vs. Temperature

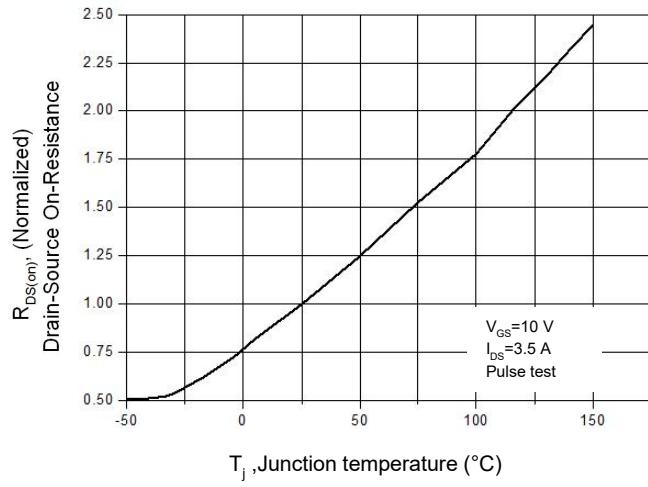


Figure 7. Capacitance Characteristics

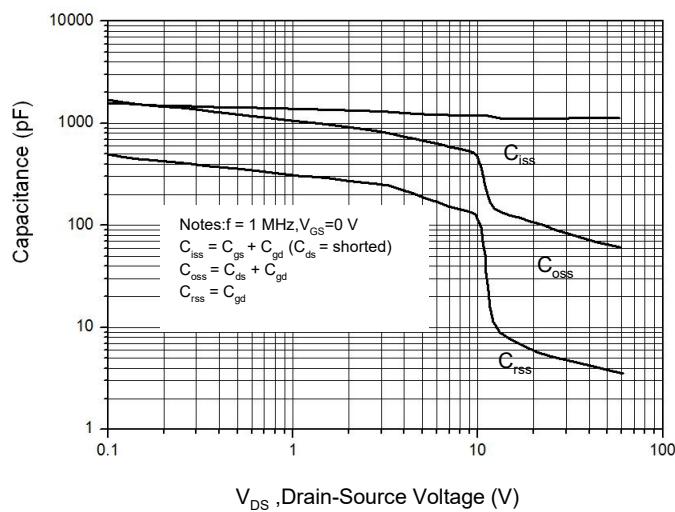


Figure 9. Maximum Safe Operating Area

TO-220F

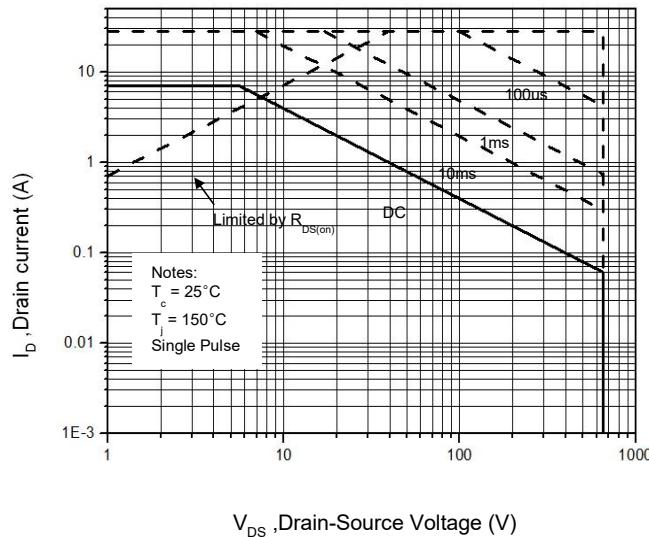


Figure 11. Power Dissipation vs. Temperature

TO-220F

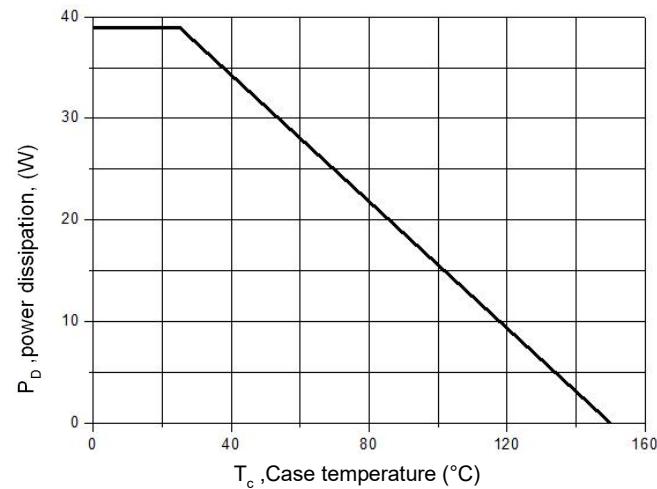


Figure 8. Gate Charge Characterist

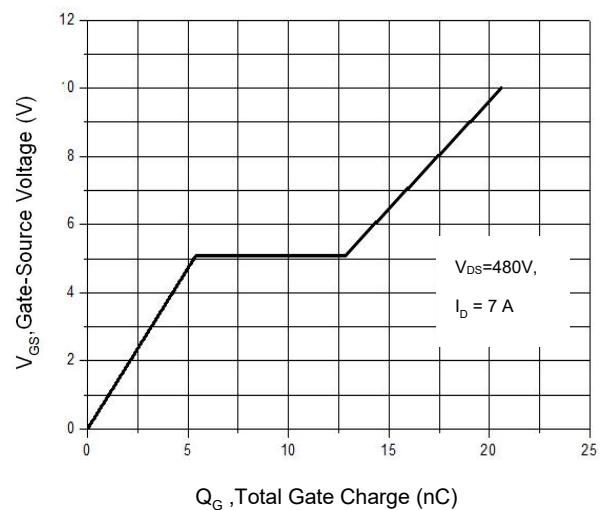


Figure 10. Maximum Safe Operating Area

TO-220/ TO-252

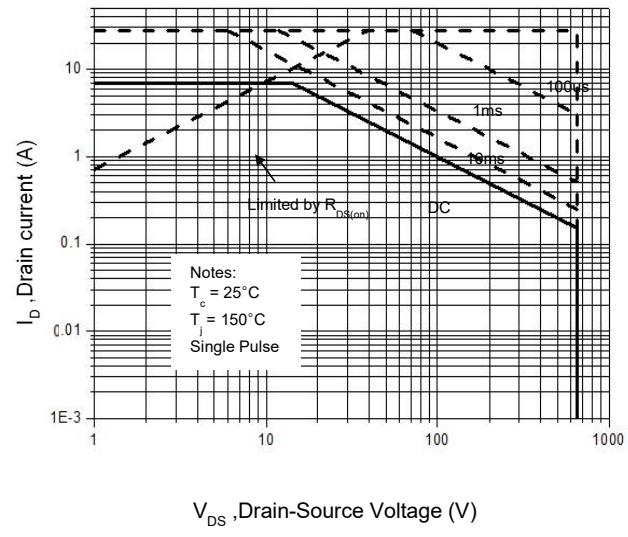


Figure 12. Power Dissipation vs. Temperature

TO-220 / TO-252

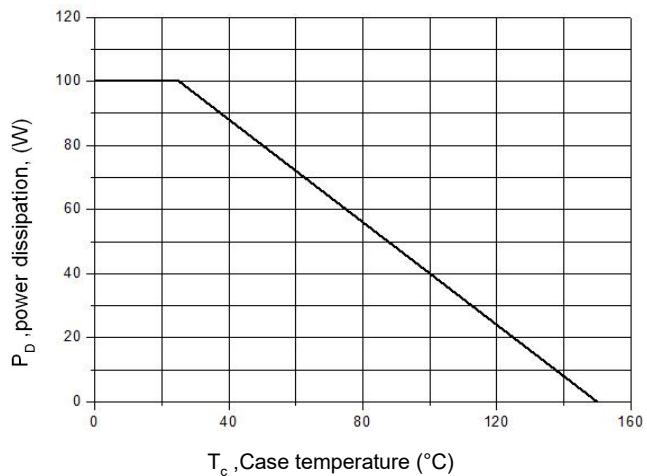


Figure 13. Continuous Drain Current vs. Temperature

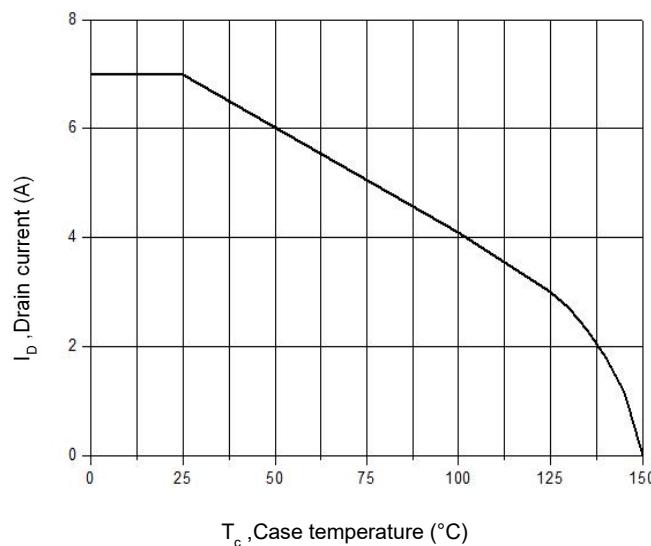


Figure 14. Body Diode Transfer Characteristics

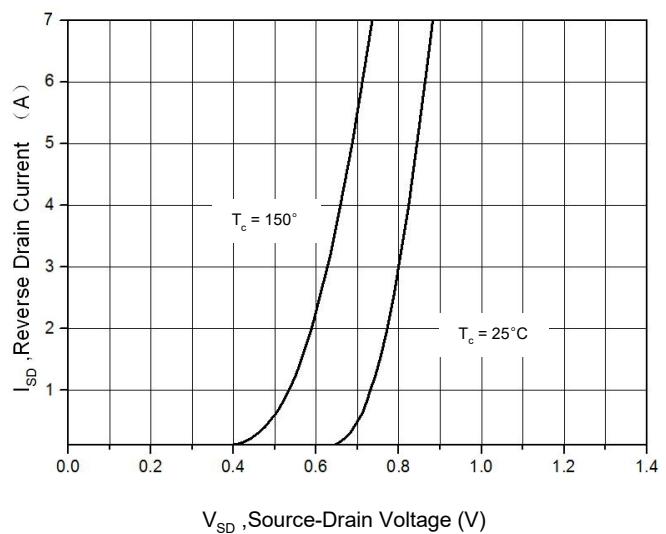


Figure 15 Transient Thermal Impedance,Junction to Case, TO-220F

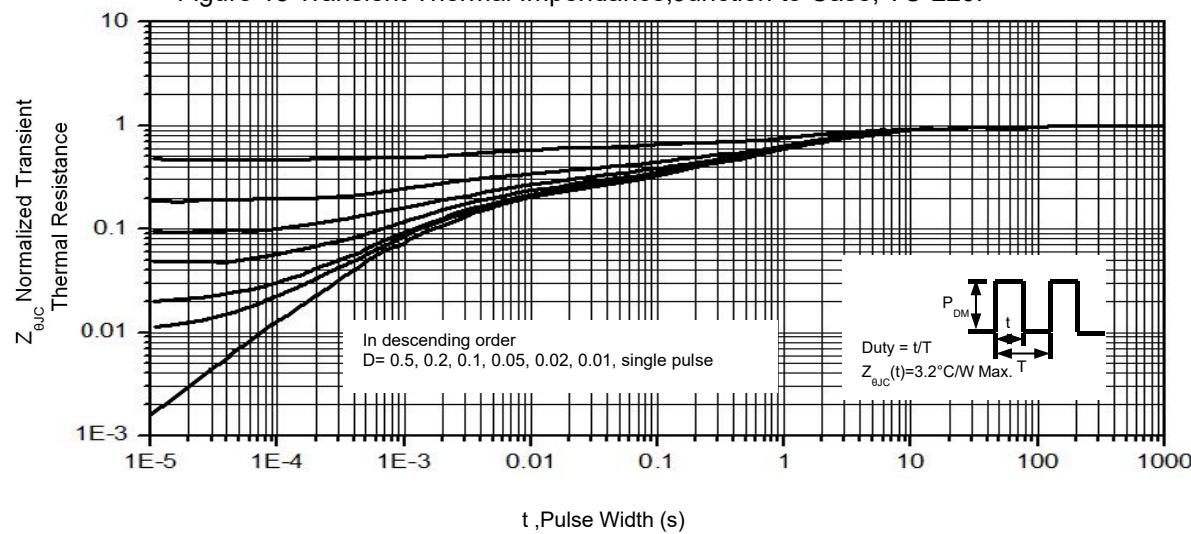
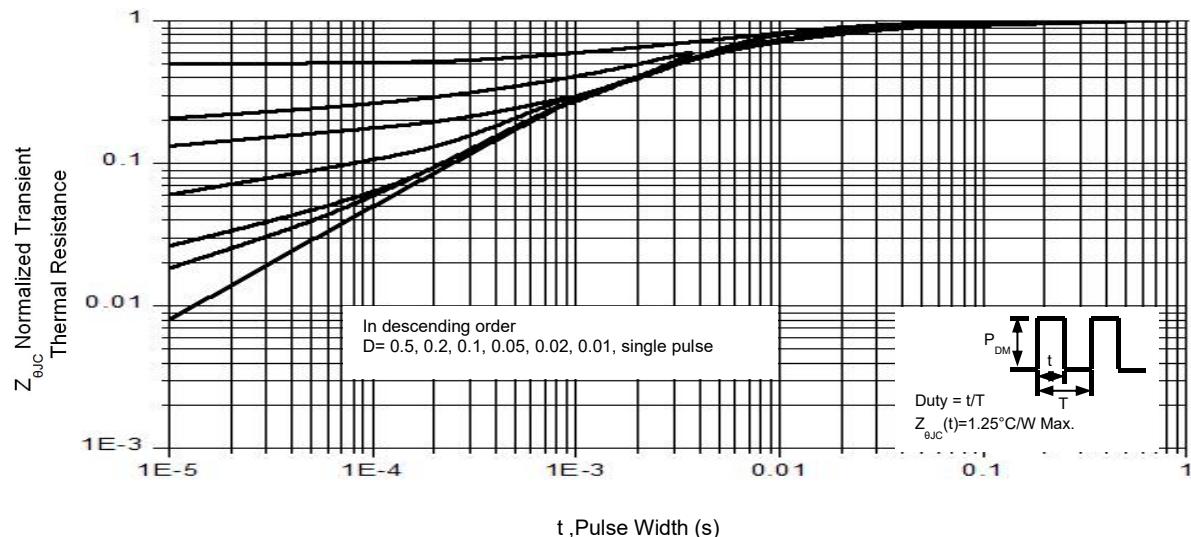
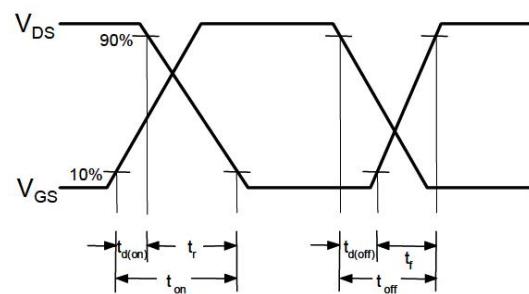
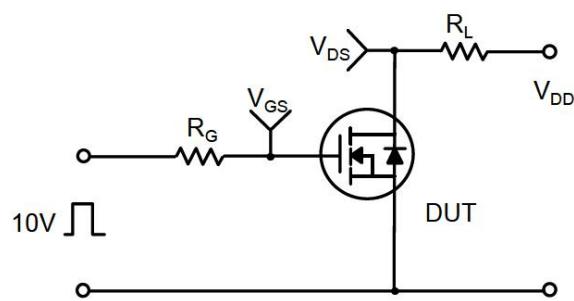
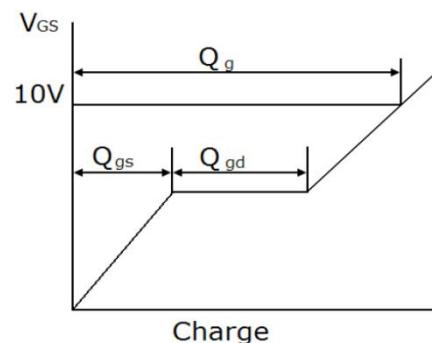
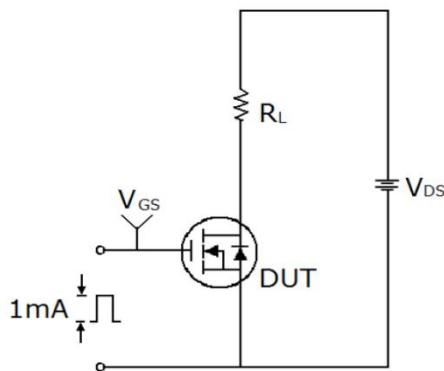


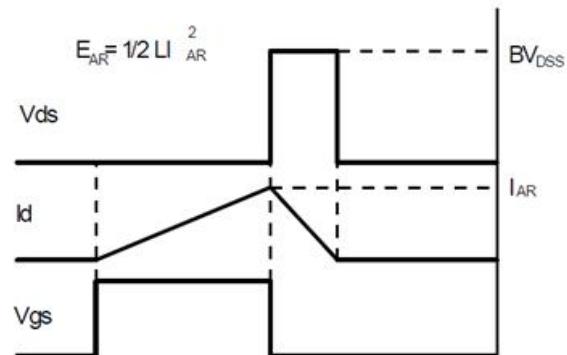
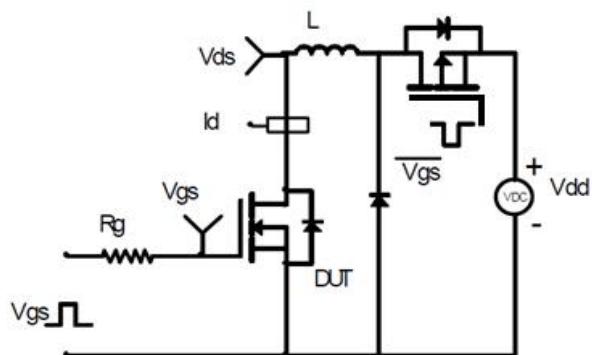
Figure 16. Transient Thermal Impedance,Junction to Case, TO-220/ TO-252



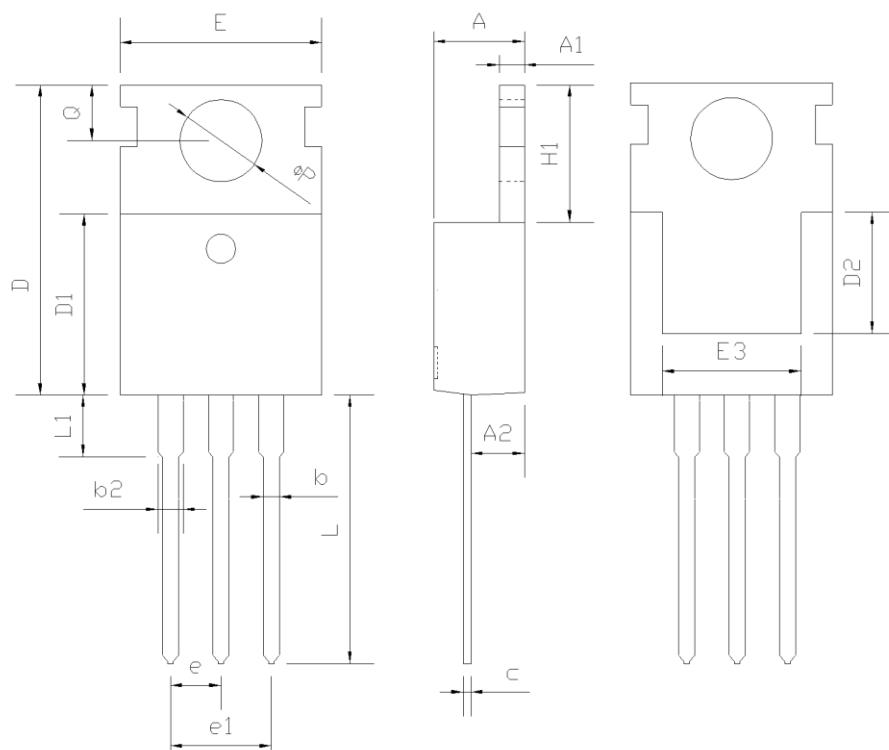
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveforms

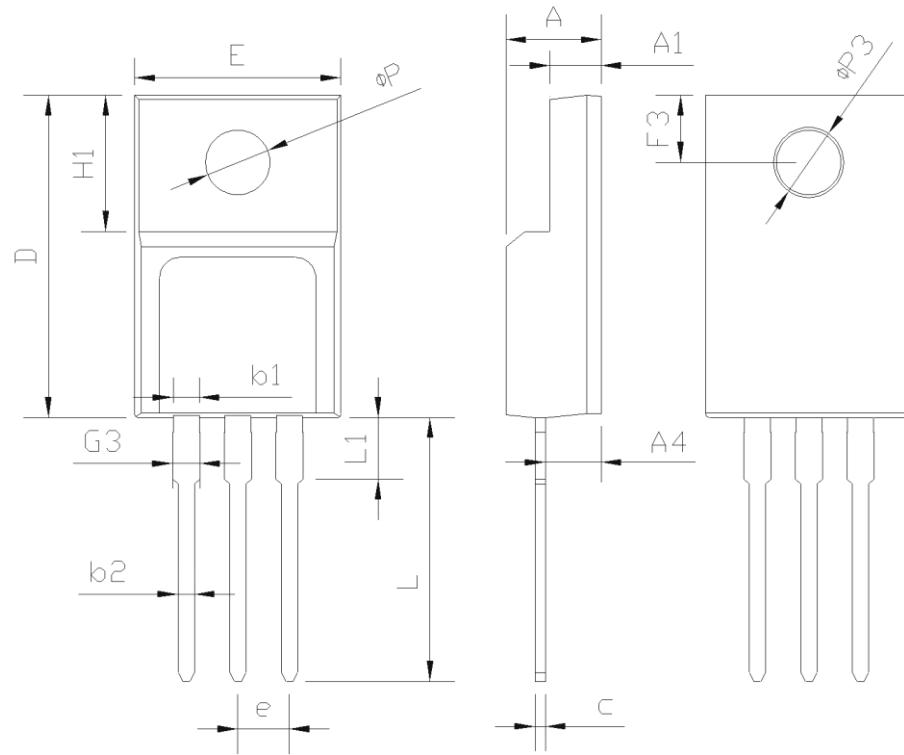


Mechanical Dimensions for TO-220



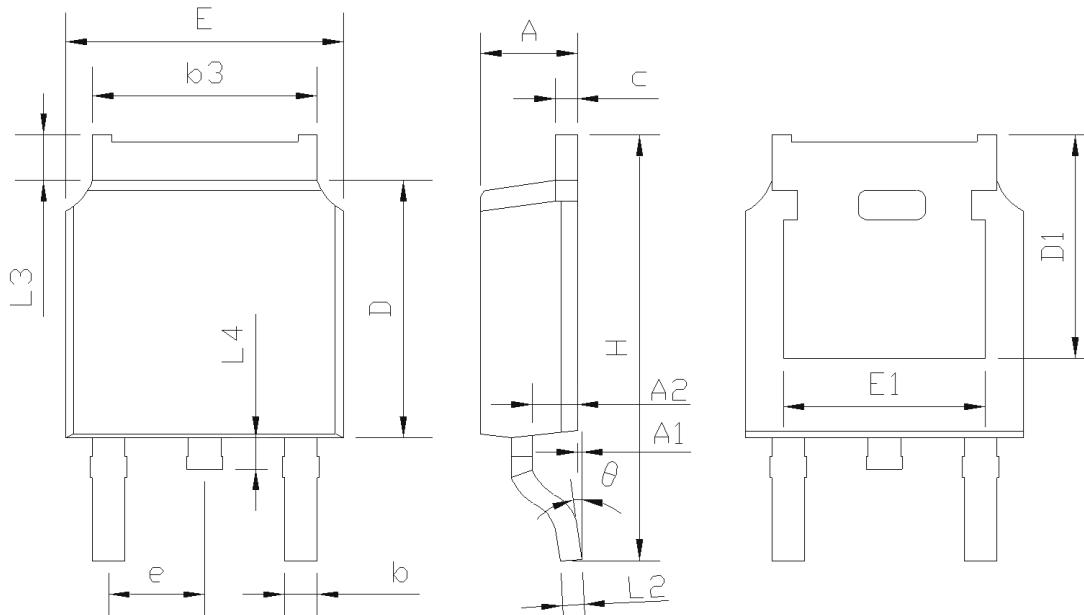
SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00

Mechanical Dimensions for TO-220F



SYMBOL	mm		
	MIN	NOM	MAX
E	9.96	10.16	10.36
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A4	2.56	2.76	2.96
c	0.40	0.50	0.65
D	15.57	15.87	16.17
H1	6.70REF		
e	2.54BSC		
L	12.68	12.98	13.28
L1	2.88	3.03	3.18
φP	3.03	3.18	3.38
φP3	3.15	3.45	3.65
F3	3.15	3.30	3.45
G3	1.25	1.35	1.55
b1	1.18	1.28	1.43
b2	0.70	0.80	0.95

Mechanical Dimensions for TO-252



SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
θ	0°	-	8°

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