

JMW

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The Power MOSFET is fabricated using the advanced planer VDMOS technology. The resulting device has low conduction resistance, superior switching performance and high avalanche energy.

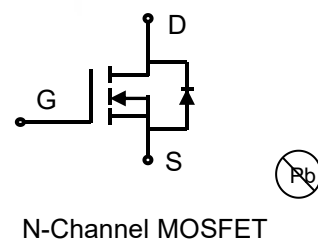
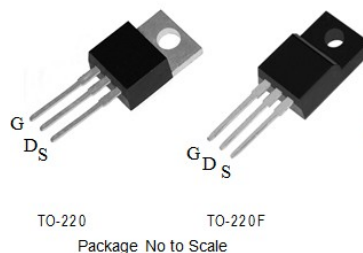
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- ◆ Low $R_{DS(on)}$
- ◆ Low gate charge (typ. $Q_g = 58.3$ nC)
- ◆ 100% UIS tested
- ◆ RoHS compliant

A

- ◆ Power factor correction.
- ◆ Switched mode power supplies.
- ◆ LED driver.

V_{DSS}	650V
I_D	20A
$R_{DS(on),max}$	0.5 Ω
$Q_{g,typ}$	58.3 nC



N-Channel MOSFET

A M

Drain-Source Voltage	V_{DSS}	650	V
Continuous drain current ($T_C = 25^\circ\text{C}$)	I_D	20	A
($T_C = 100^\circ\text{C}$)		12.5	A
Pulsed drain current ¹⁾	I_{DM}	80	A
Gate-Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse ²⁾	E_{AS}	720	mJ
Peak diode recovery dv/dt ³⁾	dv/dt	5	V/ns
Power Dissipation TO-220F ($T_C = 25^\circ\text{C}$)	P_D	45	W
Derate above 25°C		0.36	W/ $^\circ\text{C}$
Power Dissipation TO-220 ($T_C = 25^\circ\text{C}$)	P_D	250	W
Derate above 25°C		2	W/ $^\circ\text{C}$
Operating junction and storage temperature range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Continuous diode forward current	I_S	20	A
Diode pulse current	$I_{S,pulse}$	80	A

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Thermal resistance, Junction-to-case	$R_{\theta JC}$	2.78	0.5	$^\circ\text{C/W}$
Thermal resistance, Junction-to-ambient	$R_{\theta JA}$	62.5	40	$^\circ\text{C/W}$

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		M		
JMF20N65C	TO-220F	JMF20N65C	50	
JMA20N65C	TO-220	JMA20N65C	50	

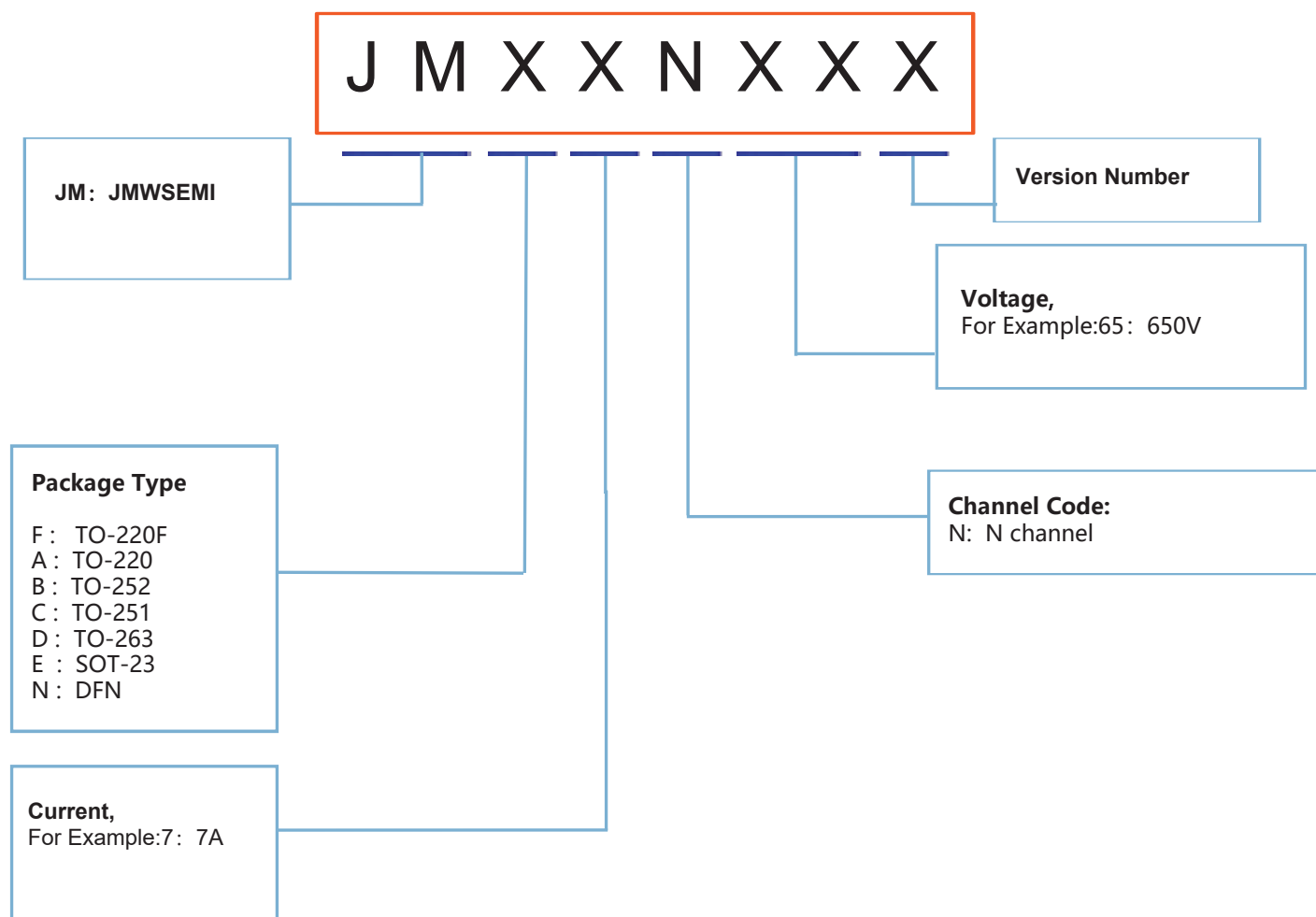
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 $T_c = 25^{\circ}\text{C}$ unless otherwise noted

		C	M		M	
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =0.25 mA	650	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =0.25 mA	2	-	4	V
Drain cut-off current	I _{DSS}	V _{DS} =650 V, V _{GS} =0 V, T _j = 25°C T _j = 125°C	- -	-	1 100	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =30 V, V _{DS} =0 V	-	-	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-30 V, V _{DS} =0 V	-	-	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =10A	-	0.42	0.5	Ω
Input capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	2962	-	pF
Output capacitance	C _{oss}		-	266	-	
Reverse transfer capacitance	C _{rss}		-	18	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 325 V, I _D = 20A R _G = 10 Ω, V _{GS} =15 V	-	18.8	-	ns
Rise time	t _r		-	43.4	-	
Turn-off delay time	t _{d(off)}		-	98.2	-	
Fall time	t _f		-	16.9	-	
G						
Gate to source charge	Q _{gs}	V _{DD} =520 V, I _D =20 A, V _{GS} =0 to 10 V	-	16.7	-	nC
Gate to drain charge	Q _{gd}		-	19.3	-	
Gate charge total	Q _g		-	58.3	-	
Gate plateau voltage	V _{plateau}		-	5	-	V
Diode forward voltage	V _{SD}	V _{GS} =0 V, I _F =20A	-	-	1.5	V
Reverse recovery time	t _{rr}	V _R =325 V, I _F =20A dI _F /dt=100 A/μs	-	492.8	-	ns
Reverse recovery charge	Q _{rr}		-	7.46	-	μC
Peak reverse recovery current	I _{rrm}		-	30.3	-	A

Notes:

1. Pulse width limited by maximum junction temperature.
2. $L=10\text{mH}$, $I_{AS} = 12\text{A}$, Starting $T_j= 25^{\circ}\text{C}$.
3. $I_{SD} = 20\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, Starting $T_j= 25^{\circ}\text{C}$.

VD MOS Product Names Rules



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Figure 1. Typical Output Characteristics

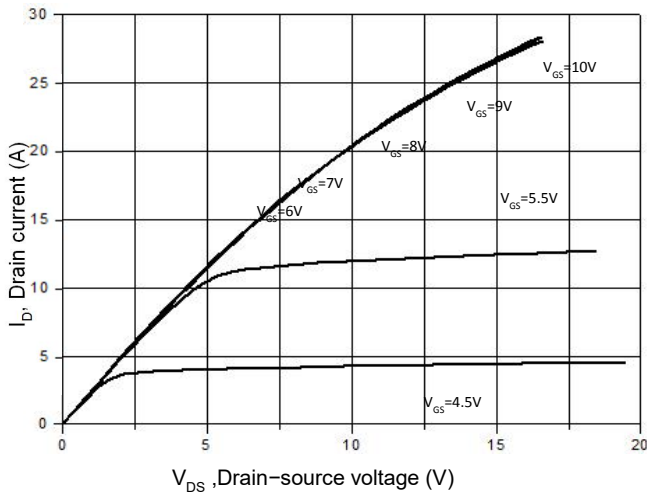


Figure 2. Transfer Characteristics

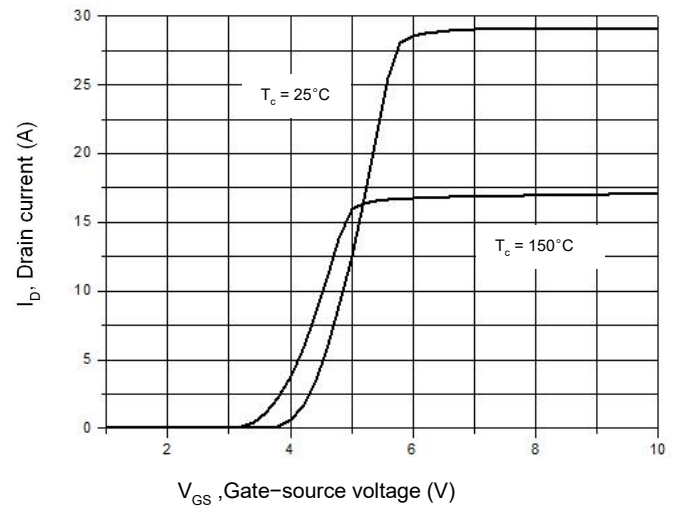


Figure 3. On-Resistance Variation vs. Drain Current

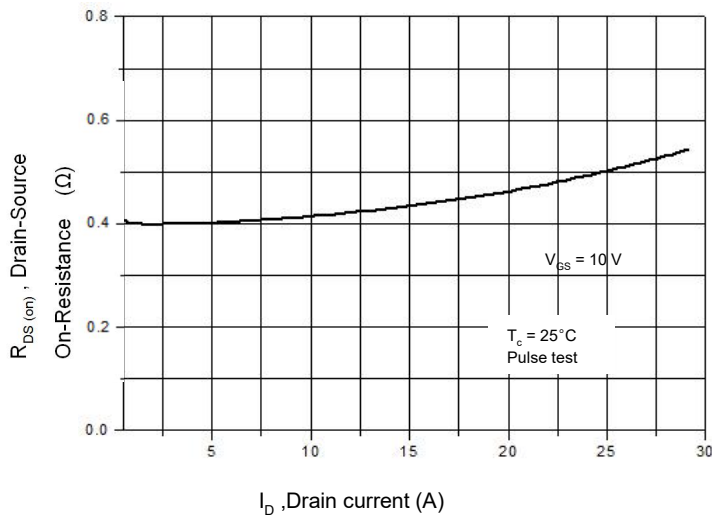


Figure 4. Threshold Voltage vs. Temperature

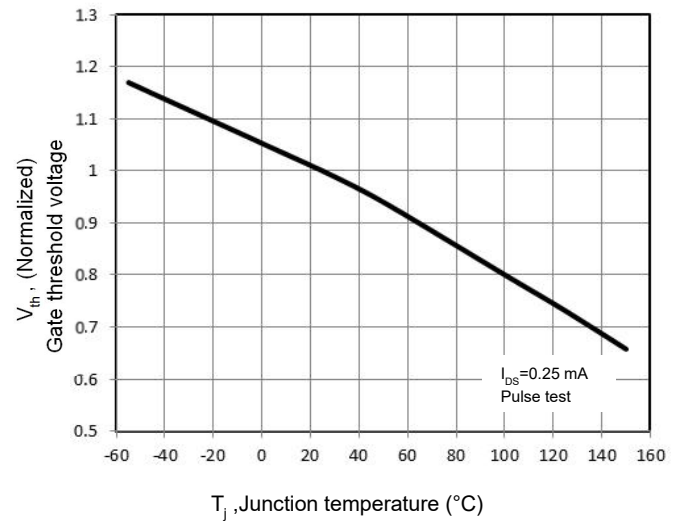


Figure 5. Breakdown Voltage vs. Temperature

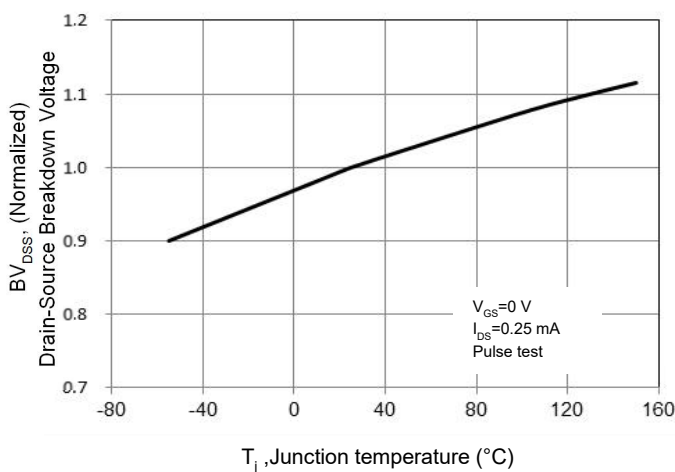


Figure 6. On-Resistance vs. Temperature

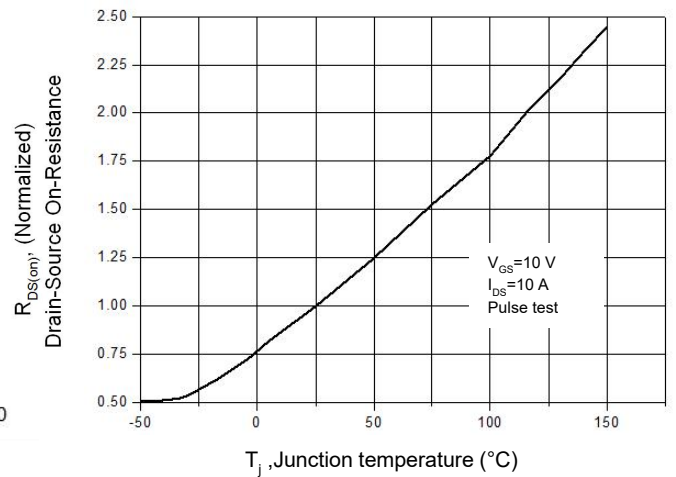


Figure 7. Capacitance Characteristics

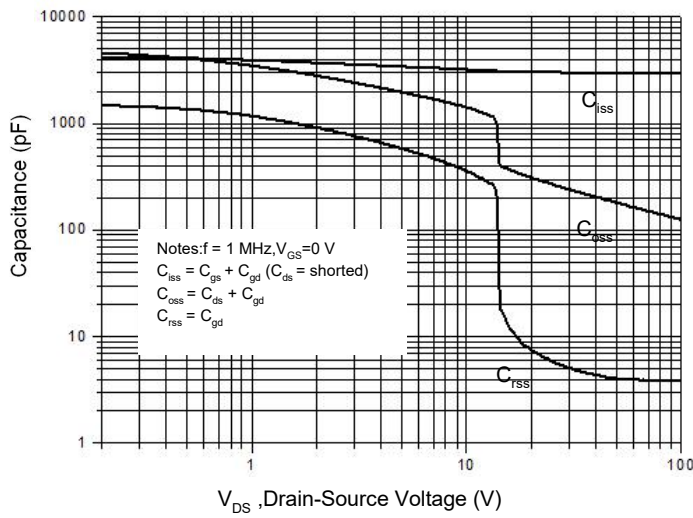


Figure 8. Gate Charge Characteristics

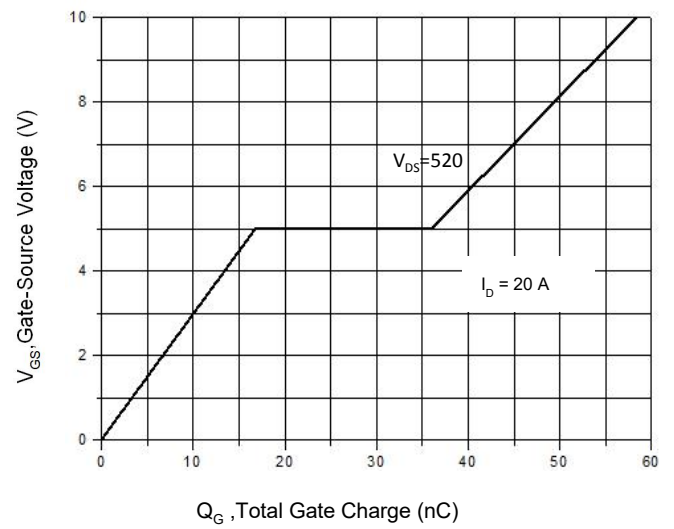


Figure 9. Maximum Safe Operating Area
TO-220F

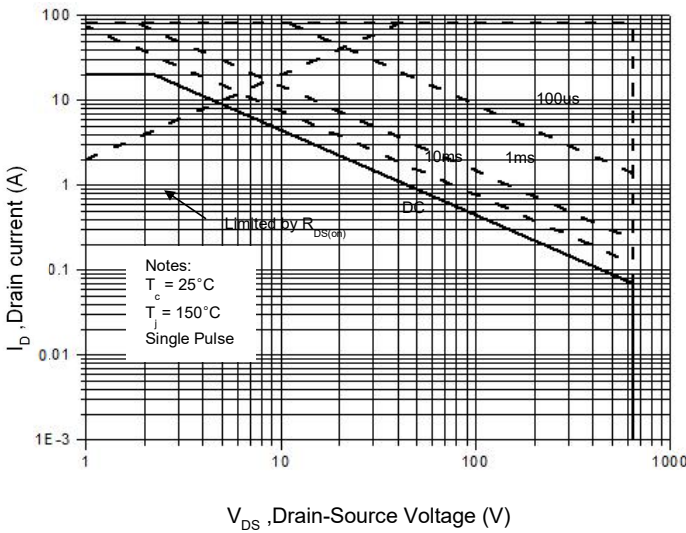


Figure 10. Maximum Safe Operating Area
TO-220

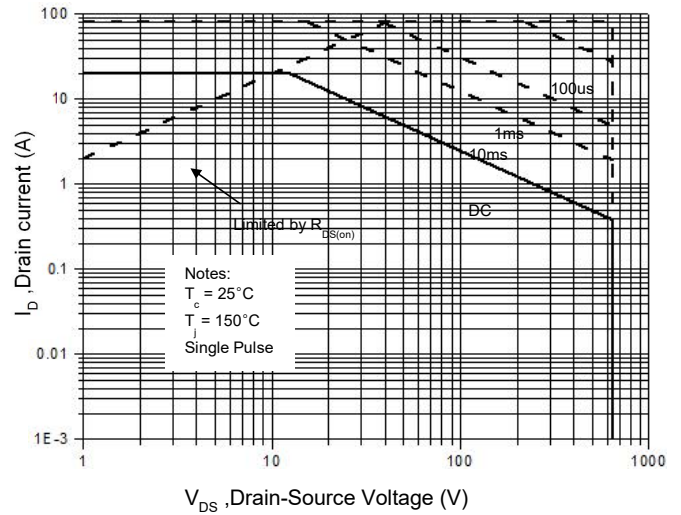


Figure 11. Power Dissipation vs. Temperature
TO-220F

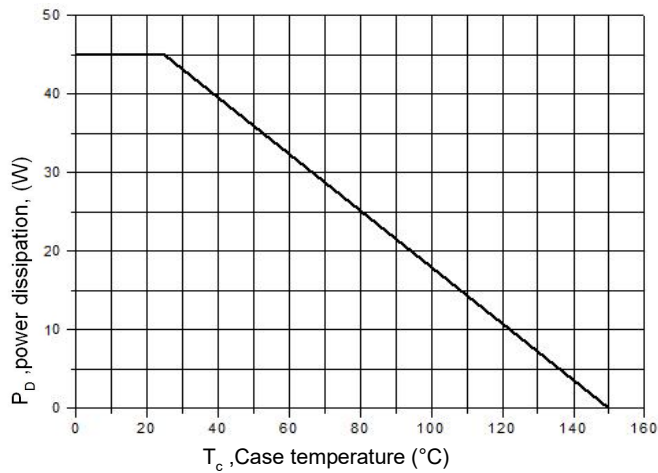


Figure 12. Power Dissipation vs. Temperature
TO-220

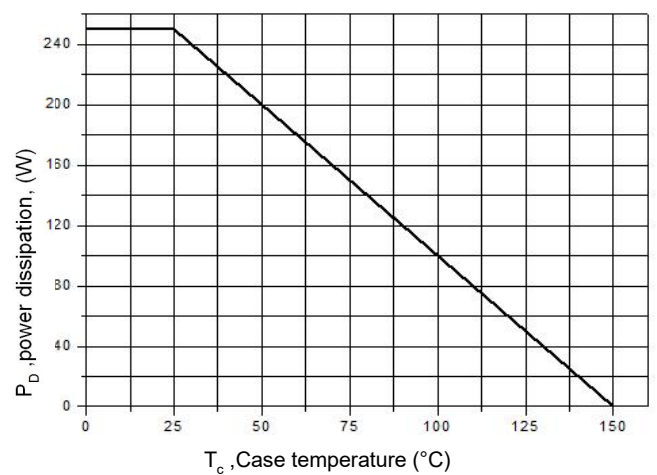


Figure 13. Continuous Drain Current vs. Temperature

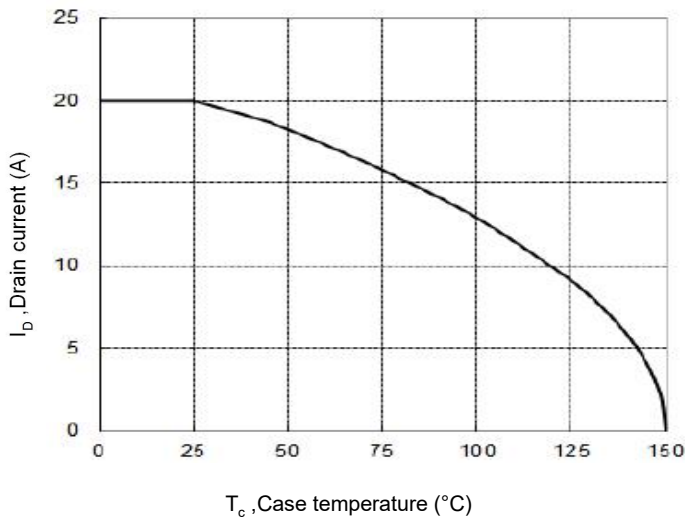


Figure 14. Body Diode Transfer Characteristics

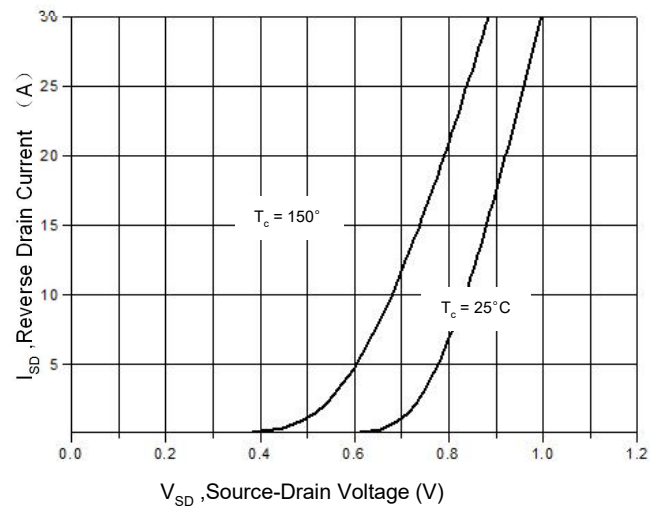


Figure 15 Transient Thermal Impedance , Junction to Case, TO-220F

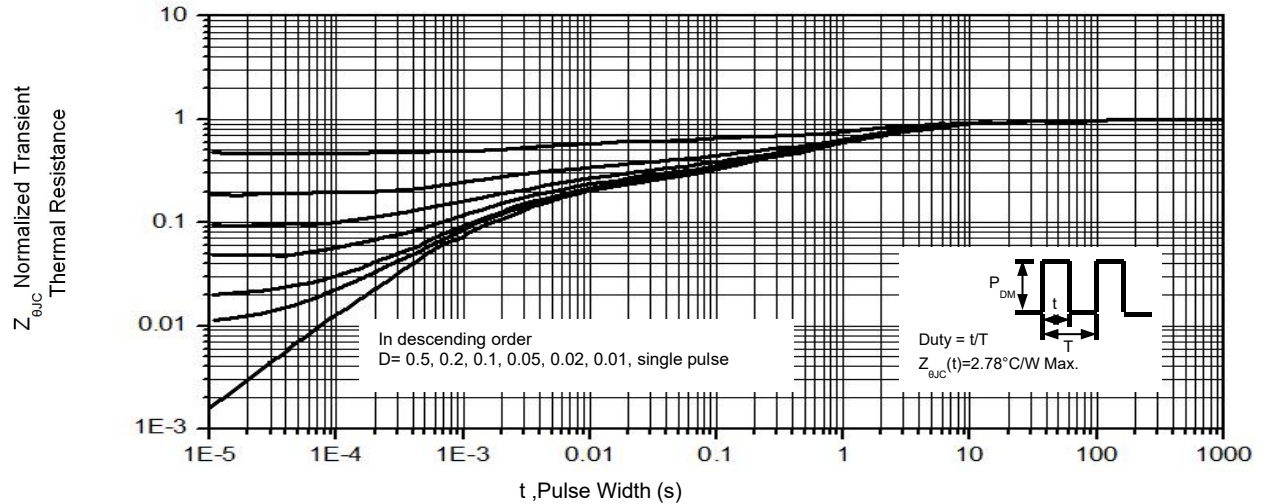
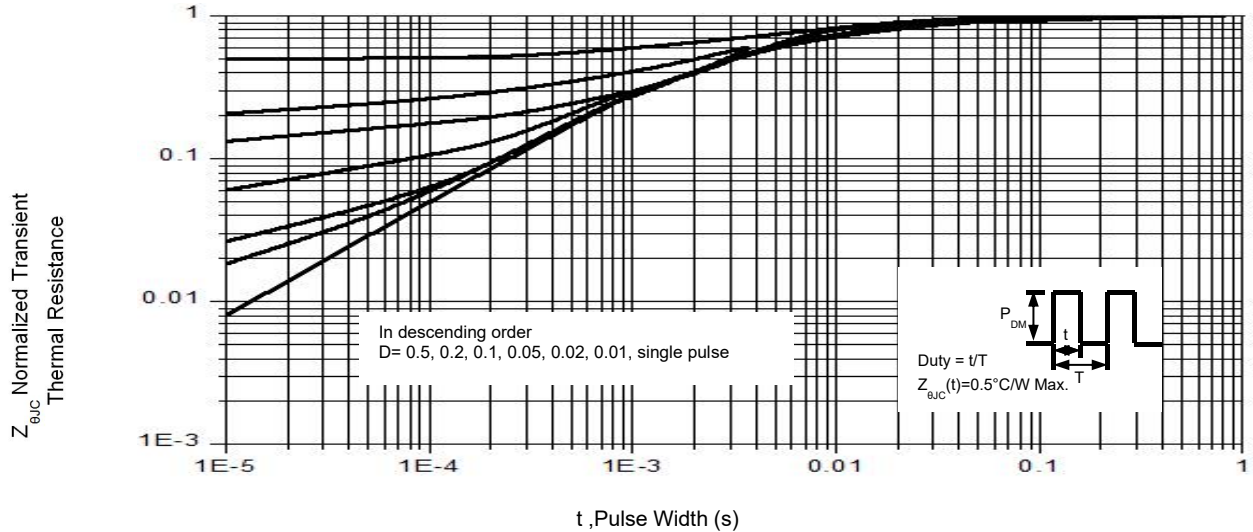
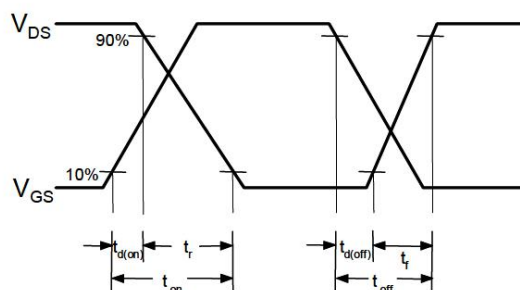
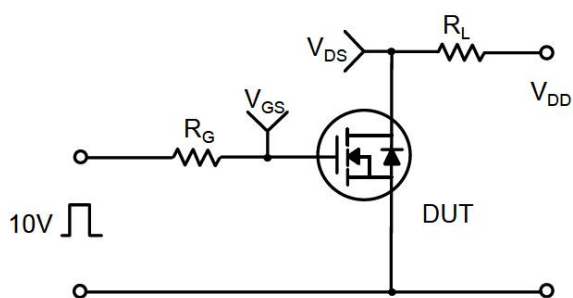
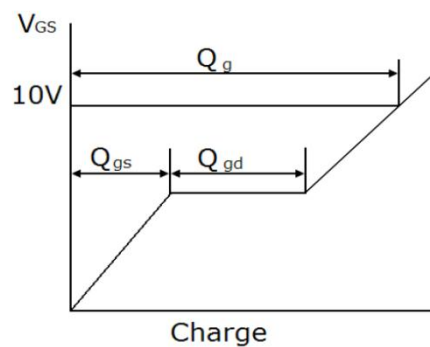
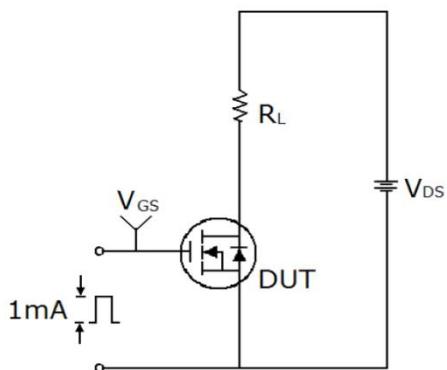


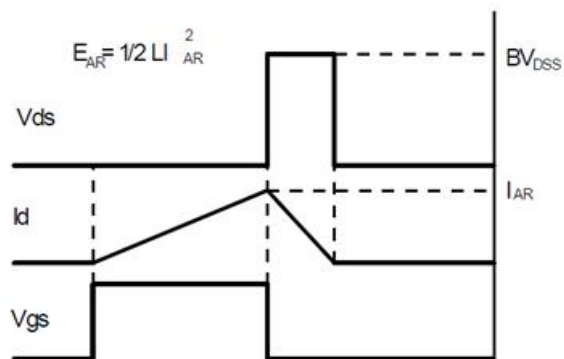
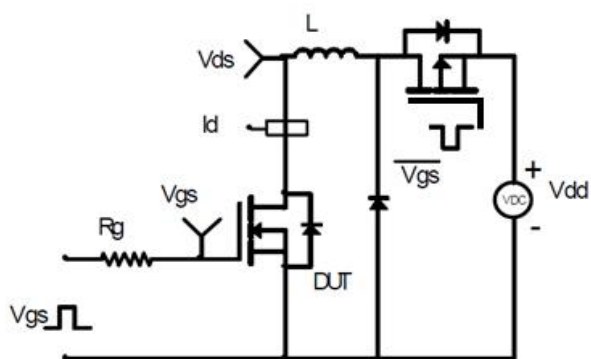
Figure 16. Transient Thermal Impedance, Junction to Case, TO-220



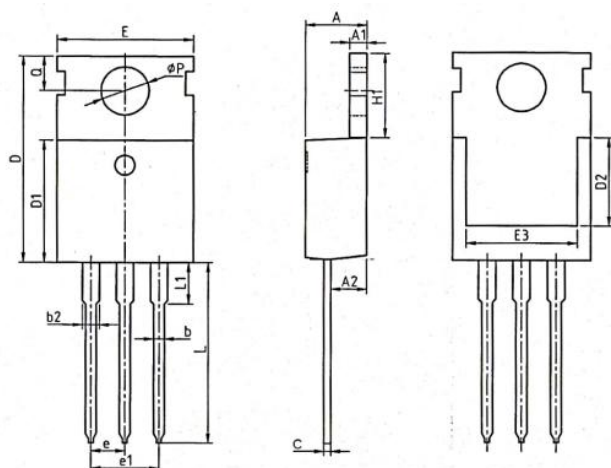
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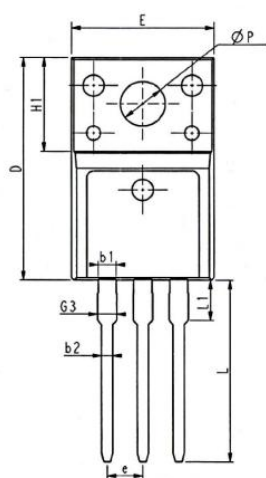


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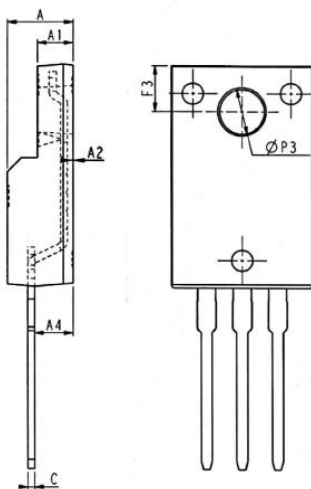


COMMON DIMENSIONS						
SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.37	4.57	4.70	0.172	0.180	0.185
A1	1.25	1.30	1.40	0.049	0.051	0.055
A2	2.20	2.40	2.60	0.087	0.094	0.102
b	0.70	0.80	0.95	0.028	0.031	0.037
b2	1.17	1.27	1.47	0.046	0.050	0.058
c	0.45	0.50	0.60	0.018	0.020	0.024
D	15.10	15.60	16.10	0.594	0.614	0.634
D1	8.80	9.10	9.40	0.346	0.358	0.370
D2	5.50	—	—	0.217	—	—
E	9.70	10.00	10.30	0.382	0.394	0.406
E3	7.00	—	—	0.276	—	—
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.25	6.50	6.85	0.246	0.256	0.270
L	12.75	13.50	13.80	0.502	0.531	0.543
L1	—	3.10	3.40	—	0.122	0.134
Øp	3.40	3.60	3.80	0.134	0.142	0.150
Q	2.60	2.80	3.00	0.102	0.110	0.118

M



F



COMMON DIMENSIONS						
SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
E	9.96	10.16	10.36	0.392	0.400	0.408
A	4.50	4.70	4.90	0.177	0.185	0.193
A1	2.34	2.54	2.74	0.092	0.100	0.108
A2	0.30	0.45	0.60	0.012	0.002	0.024
A4	2.65	2.76	2.96	0.104	0.109	0.117
C	0.40	0.50	0.65	0.016	0.020	0.026
D	15.57	15.87	16.17	0.613	0.625	0.637
H1	6.70REF			0.264REF		
e	2.54BSC			0.1BSC		
ØP	3.03	3.18	3.38	0.119	0.125	0.133
L	12.68	12.98	13.28	0.499	0.511	0.523
L1	2.88	3.03	3.18	0.113	0.119	0.125
ØP3	3.15REF			0.124REF		
F3	3.15	3.30	3.45	0.124	0.130	0.136
G3	1.25	1.35	1.55	0.049	0.053	0.061
b1	1.18	1.28	1.43	0.046	0.050	0.056
b2	0.70	0.80	0.95	0.028	0.031	0.037

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