

### •General Description

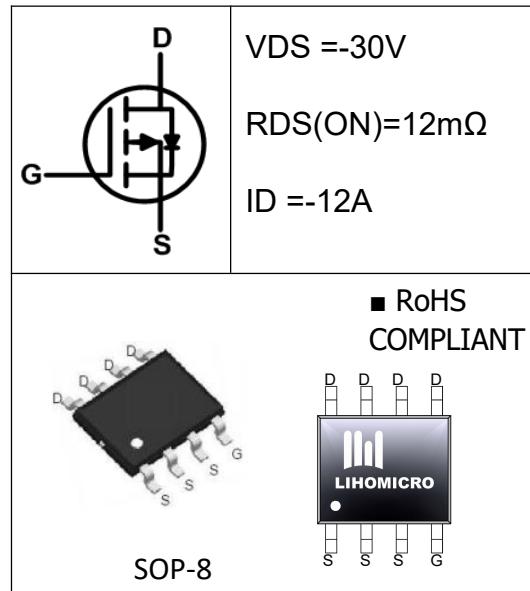
The LH4435A uses trench technology and design to provide excellent  $R_{DS(on)}$  with low gate charge. This device is suitable for high current load applications.

### •Features

- Advance high cell density trench technology
- Low RDS(ON) to minimize conductive loss
- Low Gate Charge for fast switching

### •Application

- Lighting
- Power Supplies



### •Ordering Information:

Part Number	JMP4435A
Package	SOP-8
Basic Ordering Unit (pcs)	4000
Normal Package Material Ordering Code	JMP4435A-SOP8-TAP
Halogen Free Ordering Code	JMP4435A-SOP8-TAP-HF

### •Absolute Maximum Ratings (TC = 25°C)

PARAMETER	SYMBOL	Value	UNIT
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current ,T <sub>C</sub> = 25°C	I <sub>D</sub>	-12	A
Pulsed drain current (TC = 25°C, tp limited by Tjmax) <sup>1</sup>	I <sub>DM</sub>	-50	A
Single Pulse Avalanche Energy <sup>2</sup>	E <sub>AS</sub>	75.6	mJ
Power Dissipation <sup>3</sup>	P <sub>D</sub> (T <sub>A</sub> =25°C)	3	W
	P <sub>D</sub> (T <sub>A</sub> =70°C)	2	
Operating Temperature	T <sub>J</sub>	-55~+150	°C
Storage Temperature	T <sub>STG</sub>	-55~+150	°C

● Electronic Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	-30	--	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	-0.9	-1.5	-2.5	V
Drain-source On Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -6A$	--	9.4	12	$m\Omega$
		$V_{GS} = -4.5V, I_D = -5A$	--	14	17	
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS} = -24V, V_{GS} = 0V, T_J = 25^\circ C$	--	--	-1	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	--	--	$\pm 100$	nA
Forward Transconductance	$G_{FS}$	$V_{DS} = -5V, I_D = -20A$	--	20	--	S
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz$	--	1200	--	$pF$
Output Capacitance	$C_{oss}$		--	200	--	
Reverse transfer Capacitance	$C_{rss}$		--	150	--	
Turn-On Delay Time	$T_{d(on)}$	$V_{DD} = -15V, V_{GS} = -10V, R_G = 1\Omega, I_D = -10A$	--	11	--	$nS$
Turn-Off Delay Time	$T_{d(off)}$		--	28	--	
Turn-On Rise Time	$T_r$		--	6	--	
Turn-Off Fall Time	$T_f$		--	10	--	
Total Gate Charge	$Q_g$	$I_D = -10A, V_{DS} = -15V, V_{GS} = -10V$	--	25	--	$nC$
Gate-to-Source Charge	$Q_{gs}$		--	3.9	--	
Gate-to-Drain Charge	$Q_{gd}$		--	4.8	--	
Continuous Diode Forward Current <sup>1</sup>	$I_s$	$V_{GS} = V_{DS} = 0V, \text{Force Current}$	--	--	-12	A
Pulsed Diode Forward Current	$I_{SM}$	--	--	--	-48	A
Diode Forward Voltage	$V_{SD}$	$T_J = 25^\circ C, I_S = -20A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Time	$trr$	$I_f = I_s, di_f/dt = 100A/\mu s$	--	12.3	--	ns
Reverse Recovery Charge	$Qrr$		--	6.3	--	$\mu C$

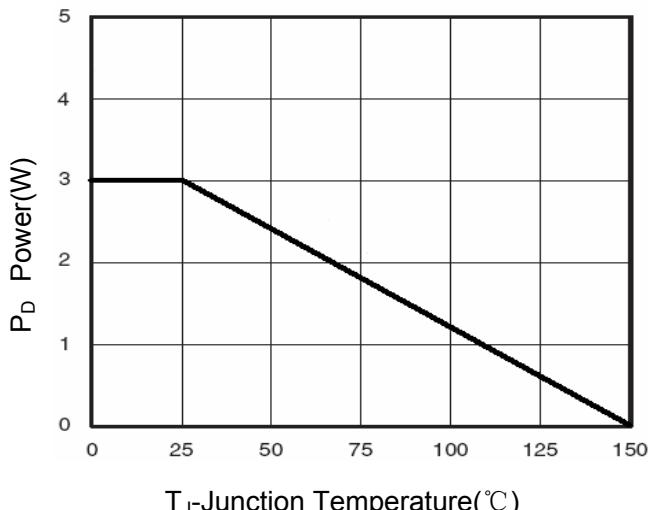
● Thermal Characteristics

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance Junction-case	$R_{thJC}$	20	$^\circ C/W$
Thermal Resistance Junction-ambient <sup>4</sup>	$R_{thJA}$	42	$^\circ C/W$

Notes:

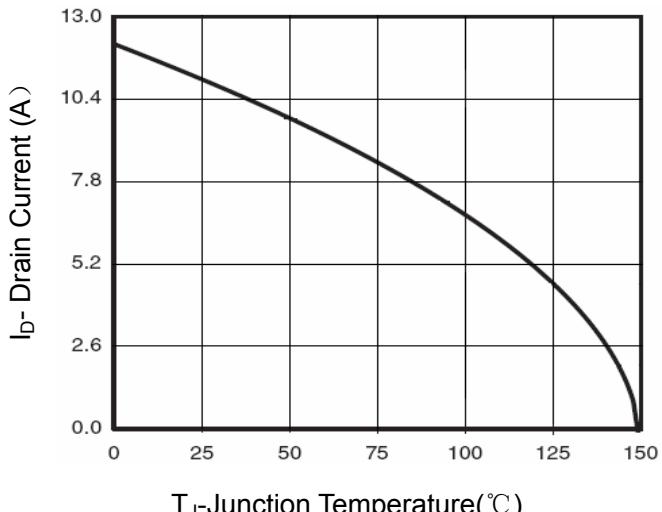
- 1.Pulse Test : Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
- 2.The EAS data shows Max. rating. The Test condition is  $L=1mH, I_D=12A, V_{DD}=-15V$ ;
- 3.The Power Dissipation is limited by  $150^\circ C$  junction temperature;
- 4.Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

•Typical Characteristics



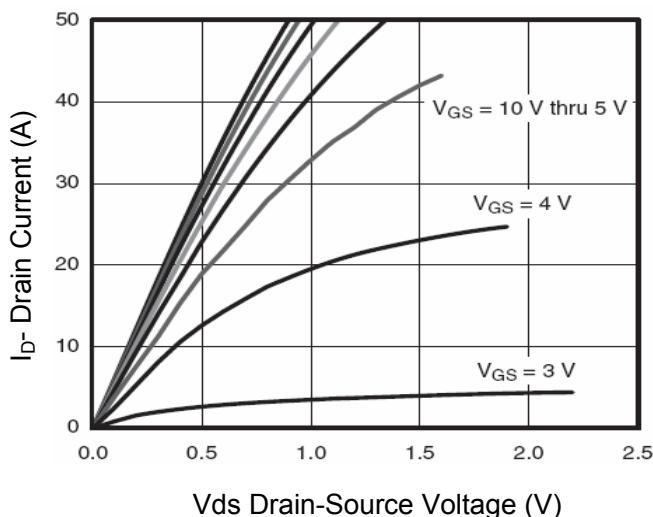
T<sub>J</sub>-Junction Temperature(°C)

**Figure 1 Power Dissipation**



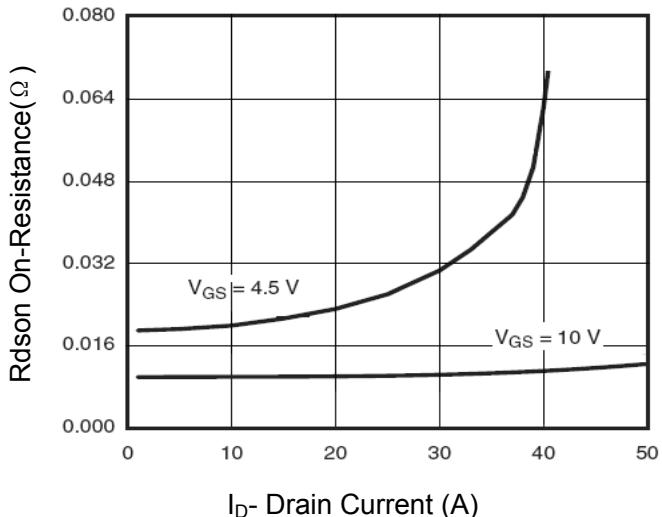
T<sub>J</sub>-Junction Temperature(°C)

**Figure 2 Drain Current**



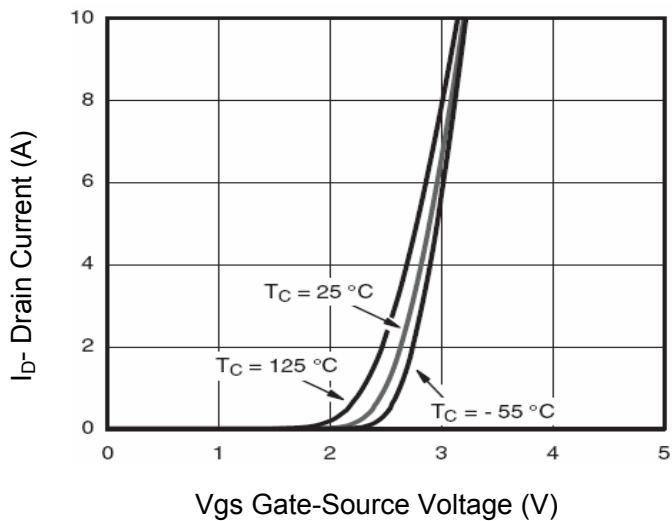
V<sub>DS</sub> Drain-Source Voltage (V)

**Figure 3 Output Characteristics**



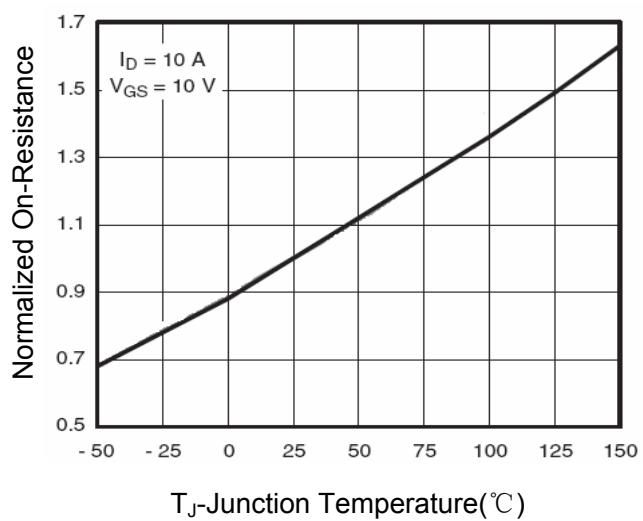
I<sub>D</sub> - Drain Current (A)

**Figure 4 Drain-Source On-Resistance**



V<sub>GS</sub> Gate-Source Voltage (V)

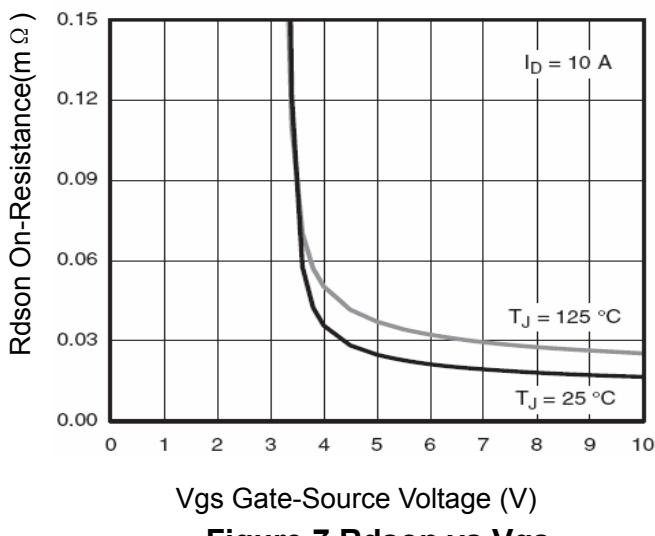
**Figure 5 Transfer Characteristics**



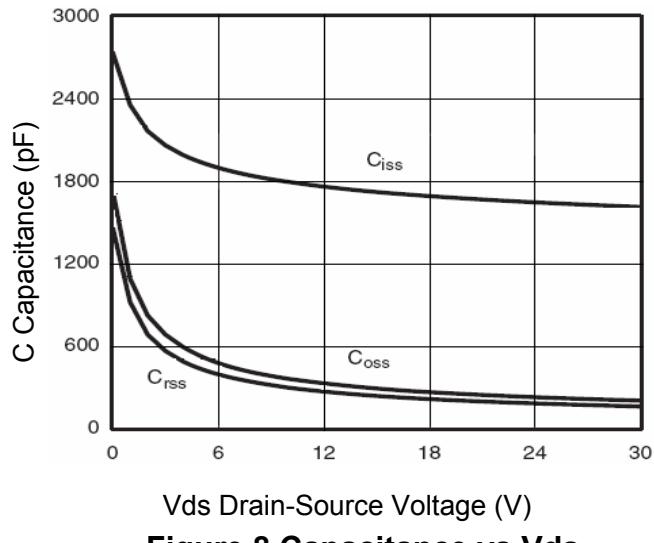
T<sub>J</sub>-Junction Temperature(°C)

**Figure 6 Drain-Source On-Resistance**

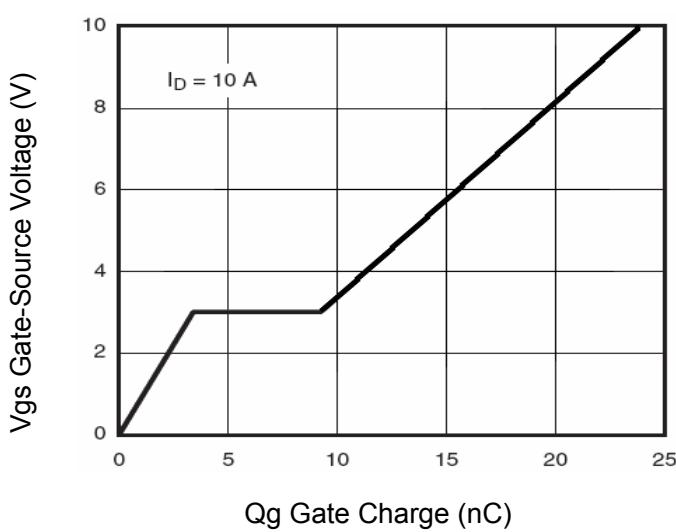
• Typical Characteristics(Cont.)



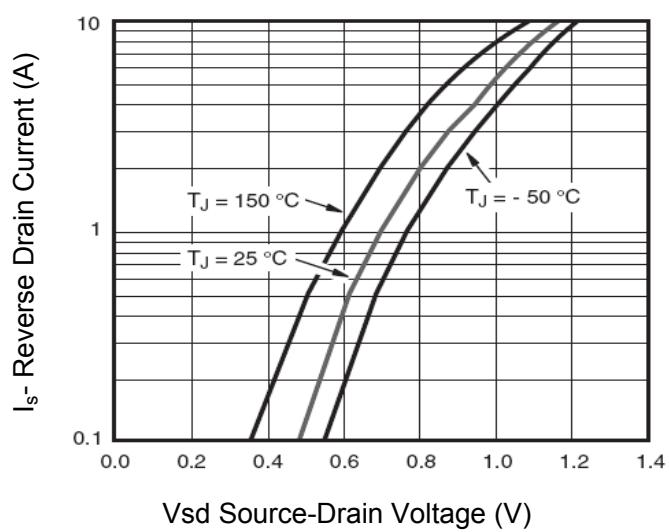
**Figure 7 Rdson vs Vgs**



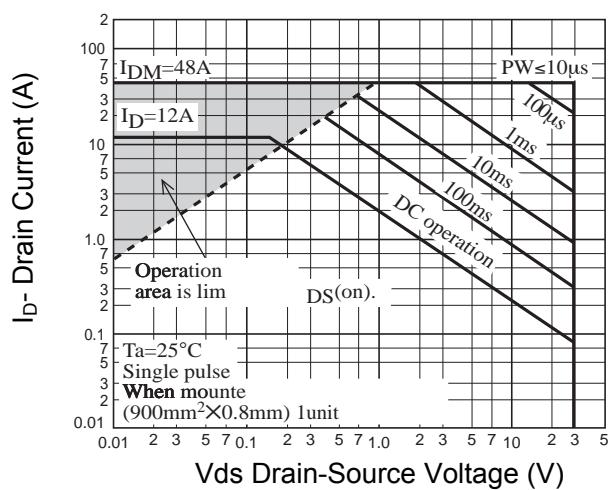
**Figure 8 Capacitance vs Vds**



**Figure 9 Gate Charge**

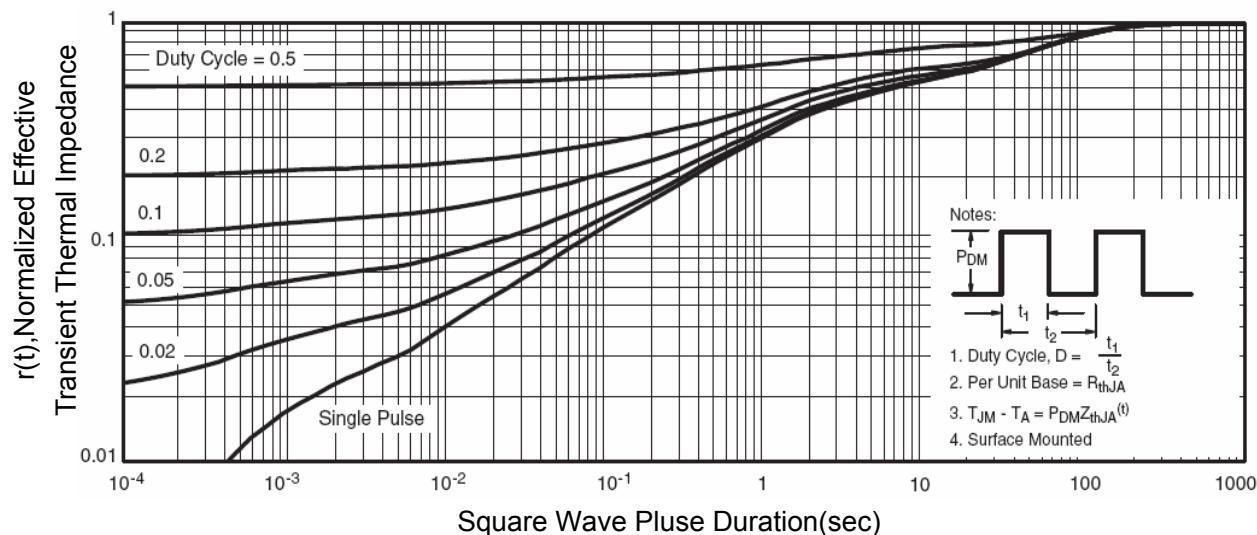


**Figure 10 Source-Drain Diode Forward**



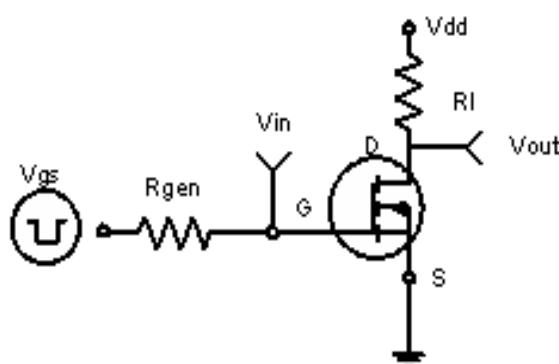
**Figure 11 Safe Operation Area**

- **Typical Characteristics(Cont.)**

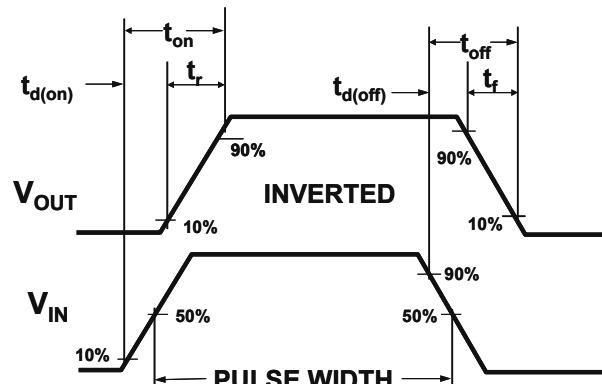


**Figure 12 Normalized Maximum Transient Thermal Impedance**

- **Test Circuits & Waveforms**



**Figure 1 Switching Test Circuit**



**Figure 2 Switching Waveforms**

## •Dimensions (SOP-8)

UNIT:mm

SYMBOL	min	max	SYMBOL	min	max
A	1.30	1.60	e	1.27BSC	
A1	1.35	1.85	L	0.40	1.30
b	0.30	0.60			
C	0.15	0.35			
D	4.60	5.20			
E	3.70	4.10			
E1	5.70	6.30			

