

General Features

- $V_{DS} = 120V$, $I_D = 90A$.
- Excellent gate charge x $R_{DS(on)}$ product(FOM).
- Very low on-resistance $R_{DS(on)}$.
- 150°C operating temperature.
- Pb-free lead plating.
- 100% UIS Tested.
- 100% ΔV_{ds} Tested.

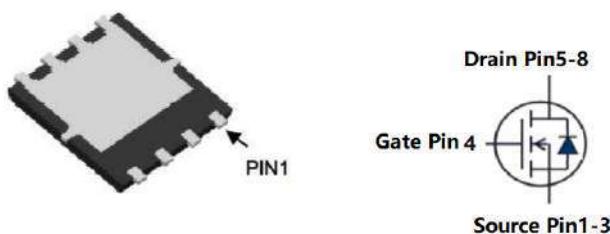
Product Summary



V_{DSS}	120	V
$R_{DS(ON)}\text{-Typ}$	5.3	$m\Omega$
I_D	90	A

Application

- DC/DC Converter.
- Hard switched and high frequency circuits.
- Ideal for high-frequency switching and synchronous rectification.



DFN5x6-8L

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	90	A
Drain Current-Continuous($T_c=100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	64	A
Pulsed Drain Current	I_{DM}	360	A
Maximum Power Dissipation	P_D	130	W
Derating factor		1.04	$\text{W}/^\circ\text{C}$
Single pulse avalanche energy ^(Note 4)	E_{AS}	400	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.96	$^\circ\text{C}/\text{W}$
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Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	120		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=120\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=45\text{A}$	-	5.3	6.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=45\text{A}$		6.5	8.0	
Forward Transconductance	g_{FS}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=50\text{A}$		60	-	S
Dynamic Characteristics ^(Note 3)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	4900	-	pF
Output Capacitance	C_{oss}		-	300	-	pF
Reverse Transfer Capacitance	C_{rss}		-	34	-	pF
Switching Characteristics ^(Note 3)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=60\text{V}, I_{\text{D}}=45\text{A}$ $V_{\text{GS}}=10\text{V}, R_{\text{G}}=1.6\Omega$	-	20	-	nS
Turn-on Rise Time	t_{r}		-	15	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	40	-	nS
Turn-Off Fall Time	t_{f}		-	10	-	nS
Total Gate Charge	Q_{g}	$V_{\text{DS}}=60\text{V}, I_{\text{D}}=45\text{A}, V_{\text{GS}}=10\text{V}$	-	90	-	nC
Gate-Source Charge	Q_{gs}		-	21	-	nC
Gate-Drain Charge	Q_{gd}		-	23.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 2)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=45\text{A}$	-	-	1.2	V
Diode Forward Current	I_{S}		-	-	90	A
Reverse Recovery Time	t_{rr}	$T_{\text{J}} = 25^\circ\text{C}, I_{\text{F}} = 45\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}$ ^(Note 3)	-	70	-	nS
Reverse Recovery Charge	Q_{rr}		-	137	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Guaranteed by design, not subject to production
4. EAS condition : $T_j=25^\circ\text{C}, V_{\text{DD}}=50\text{V}, V_{\text{G}}=10\text{V}, L=0.25\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

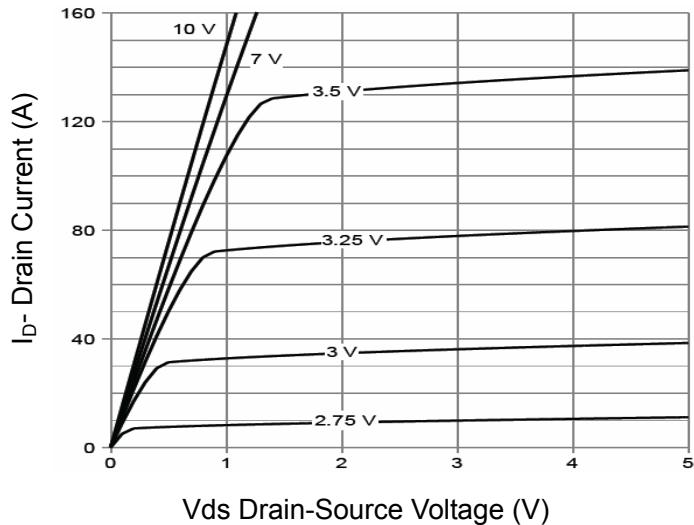


Figure 1 Output Characteristics

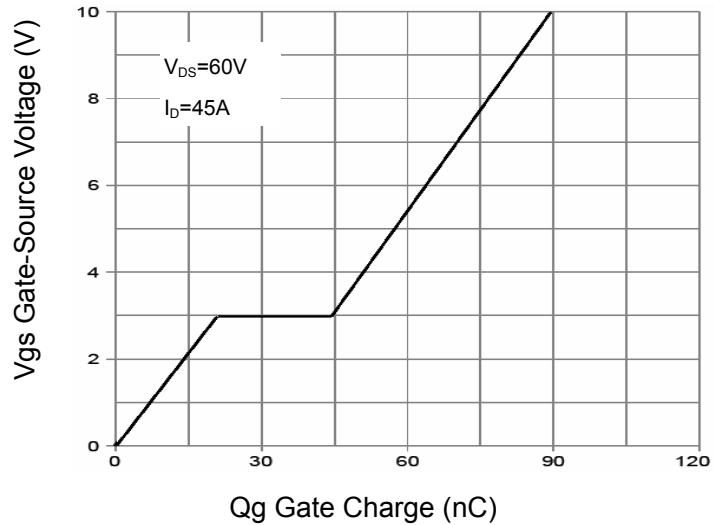


Figure 4 Gate Charge

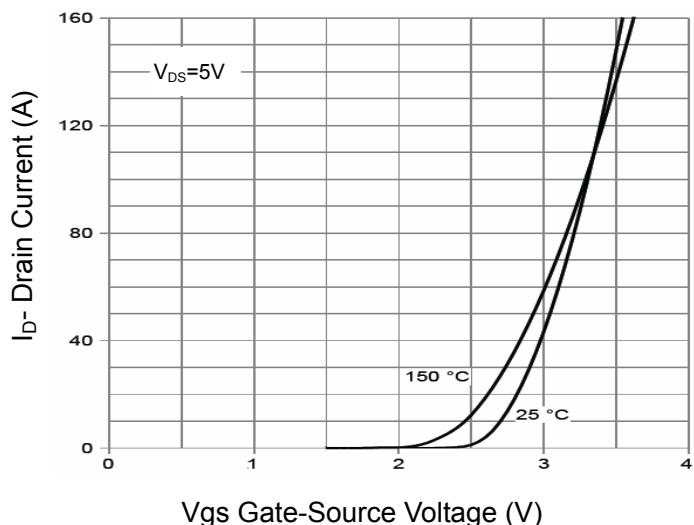


Figure 2 Transfer Characteristics

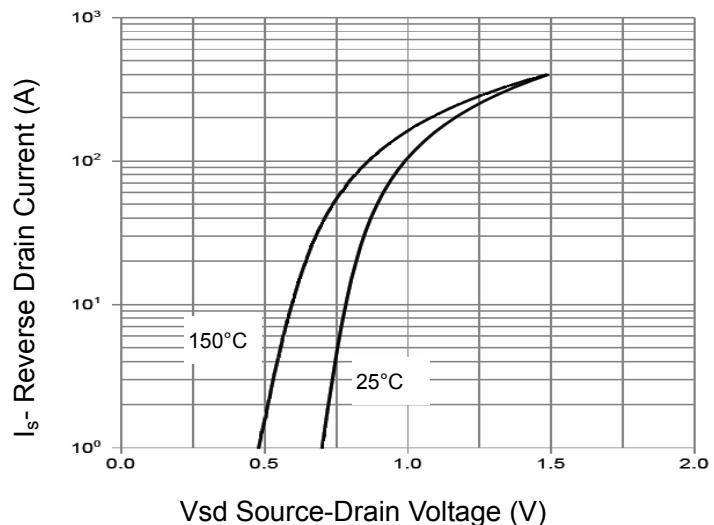


Figure 5 Source- Drain Diode Forward

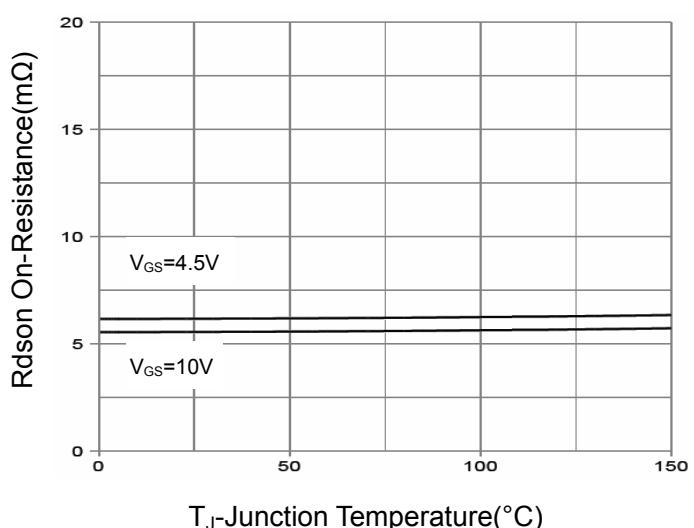


Figure 3 Rdson-Junction Temperature

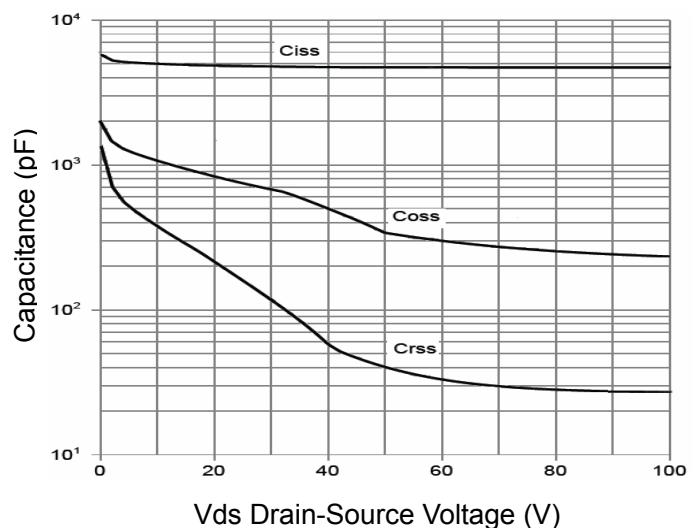


Figure 6 Capacitance vs Vds

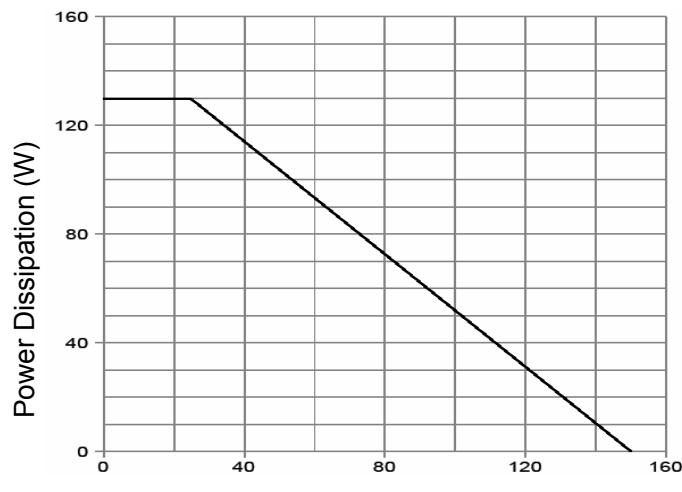


Figure 7 Power De-rating

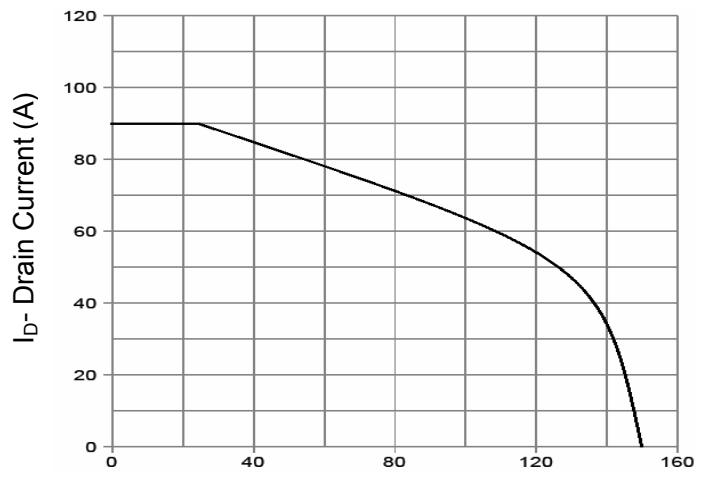


Figure 9 Current De-rating

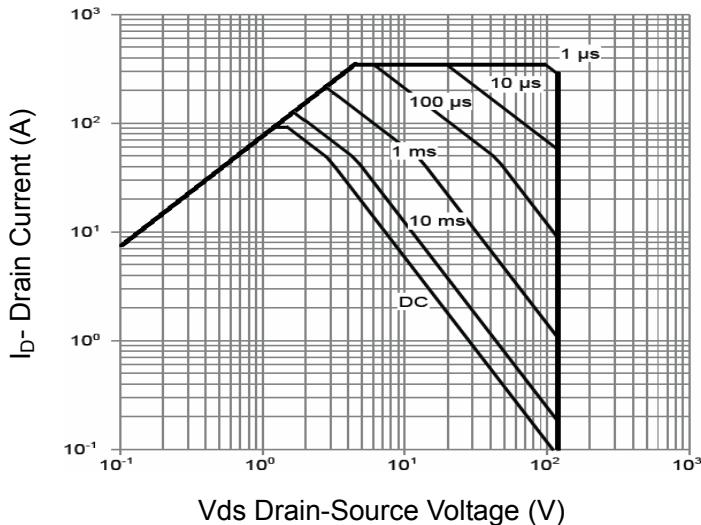


Figure 8 Safe Operation Area

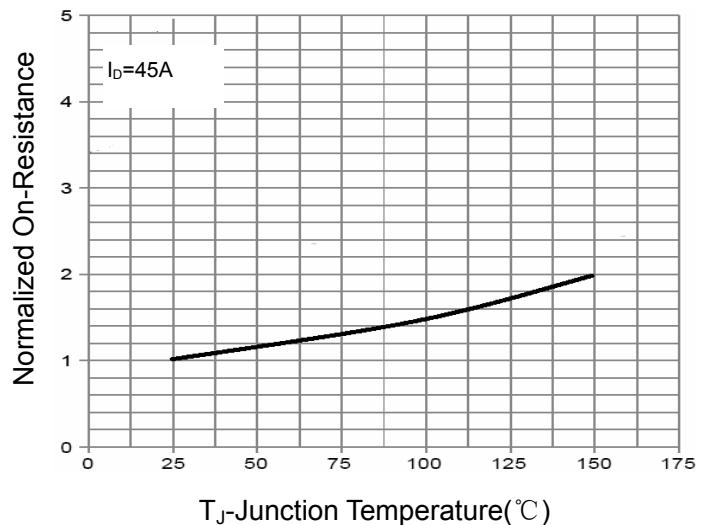


Figure 10 Rdson-Junction Temperature

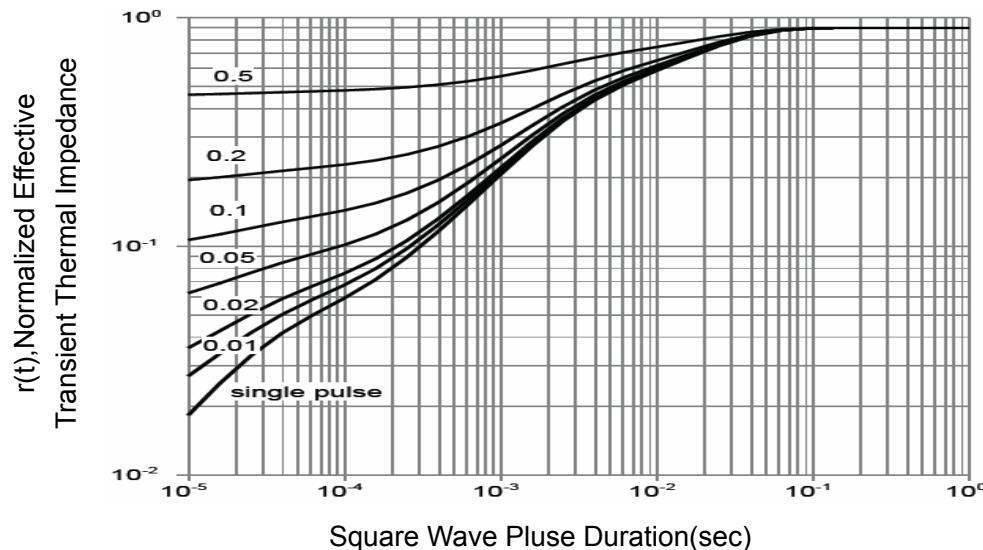


Figure 11 Normalized Maximum Transient Thermal Impedance

Test circuits

Figure 12. Switching times test circuit for resistive load

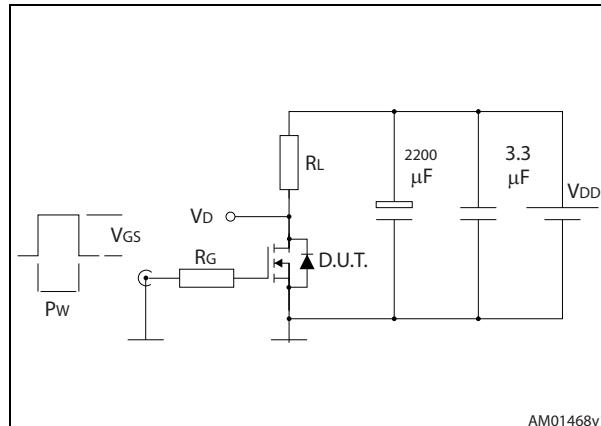


Figure 13. Gate charge test circuit

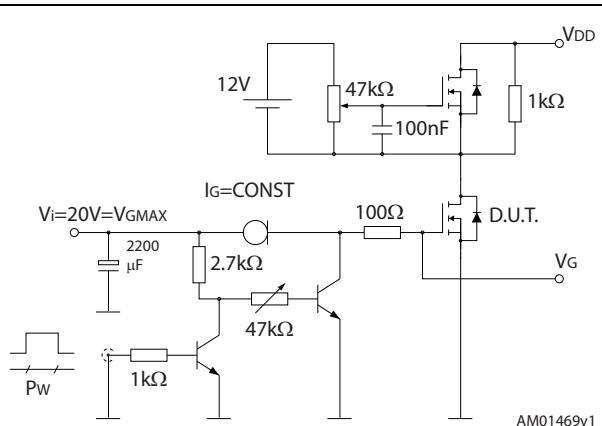


Figure 14. Test circuit for inductive load switching and diode recovery times

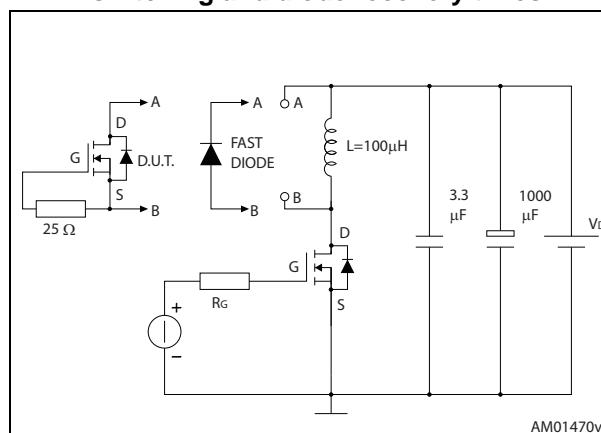


Figure 15. Unclamped inductive load test circuit

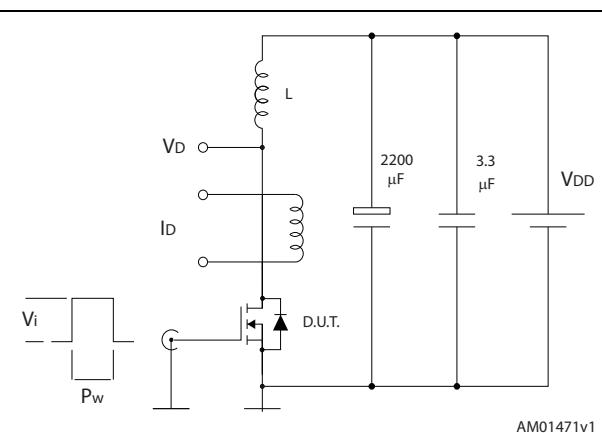


Figure 16. Unclamped inductive waveform

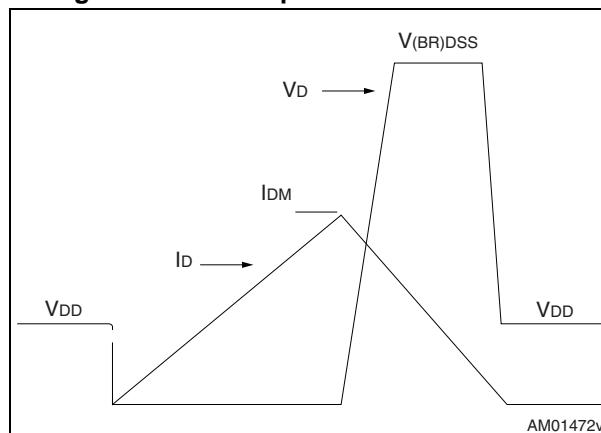
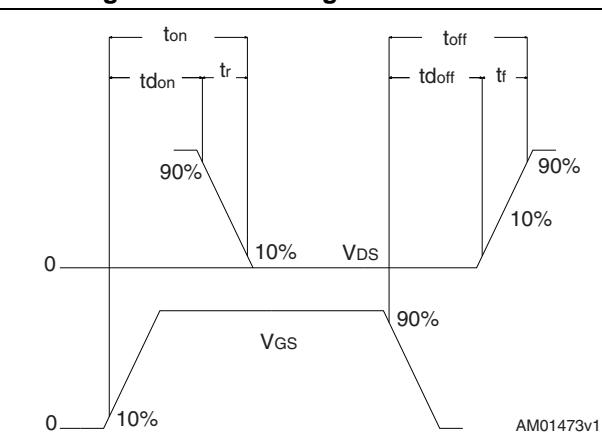
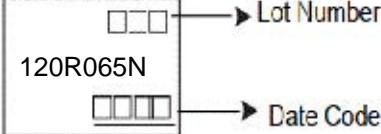


Figure 17. Switching time waveform

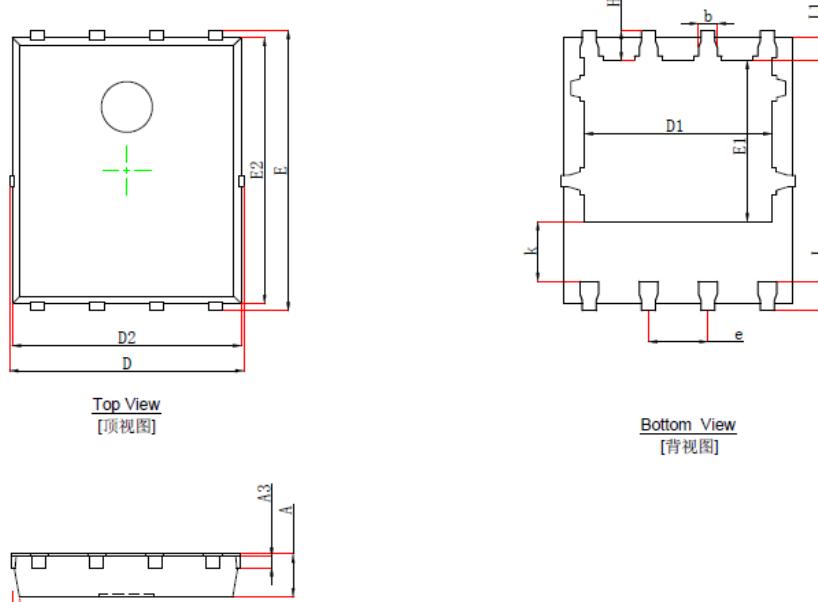


Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
JMN120R065N-R	120R065N	DFN5*6-8	Tape&Reel	5000

PACKAGE	MARKING
DFN5*6-8	

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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