

Feature

- ◇ Special process technology for high ESD capability
- ◇ High density cell design for ultra low $R_{DS(on)}$
- ◇ Fully characterized avalanche voltage and current
- ◇ Good stability and uniformity with high EAS
- ◇ Excellent package for good heat dissipation

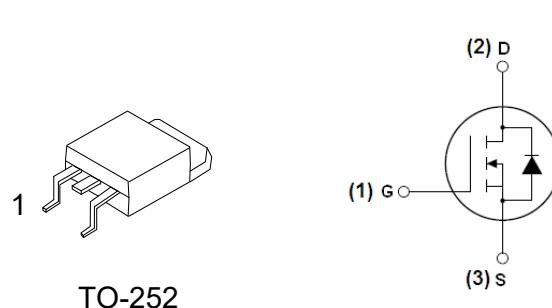
Product Summary



V_{DS}	150	V
$R_{DS(on),Max} @ V_{GS}=10\text{ V}$	26	$\text{m}\Omega$
I_D	40	A

Application

- ◇ Power switching application
- ◇ Hard switched and high frequency circuits
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control



Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	40	A
$I_D(100^\circ\text{C})$	Drain Current-Continuous($T_c=100^\circ\text{C}$)	28	A
I_{DM}	Pulsed Drain Current	88	A
P_D	Maximum Power Dissipation	98	W
	Derating factor	0.57	W/ $^\circ\text{C}$
E_{AS}	Single pulse avalanche energy ^(Note 5)	256	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	1.8	$^\circ\text{C/W}$
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Electrical Characteristics (TC=25°C unless otherwise noted)

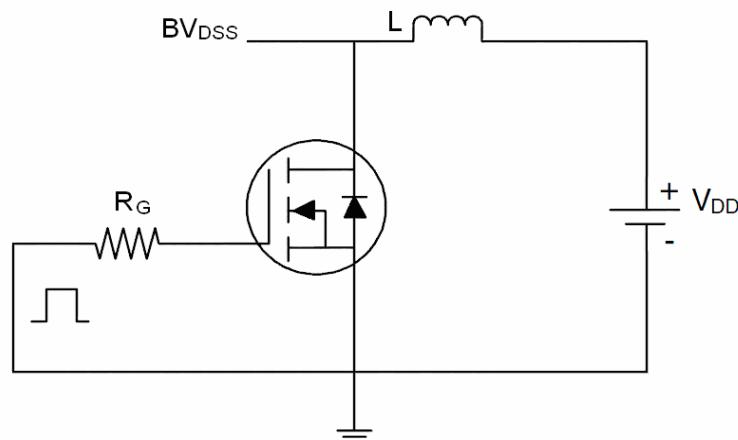
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	150	-	200	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =15A	-	23	26	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance		-	26	34	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =15A	-	15	-	S
Dynamic Characteristics ^(Note 4)						
C _{iss}	Input Capacitance	V _{DS} =75V, V _{GS} =0V, F=1.0MHz	-	2500	-	PF
C _{oss}	Output Capacitance		-	293	-	PF
C _{rss}	Reverse Transfer Capacitance		-	224	-	PF
Switching Characteristics ^(Note 4)						
t _{d(on)}	Turn-on Delay Time	V _{DD} =75V, R _L =5Ω V _{GS} =10V, R _{GEN} =3Ω	-	17	-	nS
t _r	Turn-on Rise Time		-	27	-	nS
t _{d(off)}	Turn-Off Delay Time		-	39	-	nS
t _f	Turn-Off Fall Time		-	7	-	nS
Q _g	Total Gate Charge	V _{DS} =75V, I _D =15A, V _{GS} =10V	-	39	-	nC
Q _{gs}	Gate-Source Charge		-	8	-	nC
Q _{gd}	Gate-Drain Charge		-	12	-	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage ^(Note 3)	V _{GS} =0V, I _S =15A	-	-	1.2	V
I _S	Diode Forward Current ^(Note 2)	-	-	-	40	A
t _{rr}	Reverse Recovery Time	T _J = 25°C, IF = 10A di/dt = 100A/μs ^(Note 3)	-	32	-	nS
Q _{rr}	Reverse Recovery Charge		-	53	-	nC
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

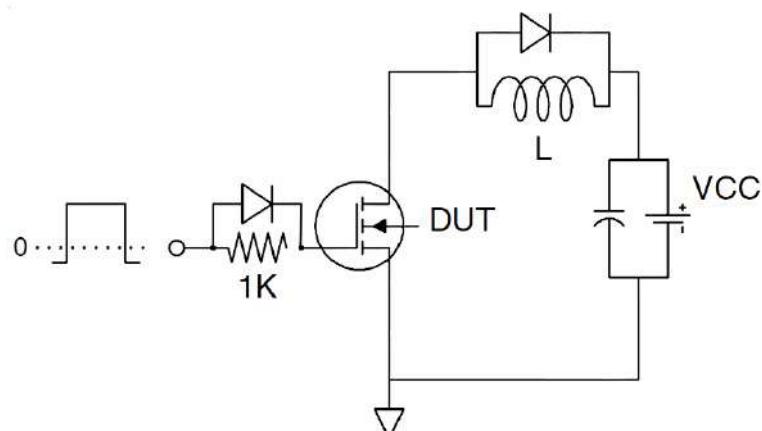
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS Condition : T_j=25°C, V_{DD}=120V, V_G=10V, L=0.5mH, R_g=25Ω, I_{AS}=32A

Test Circuit

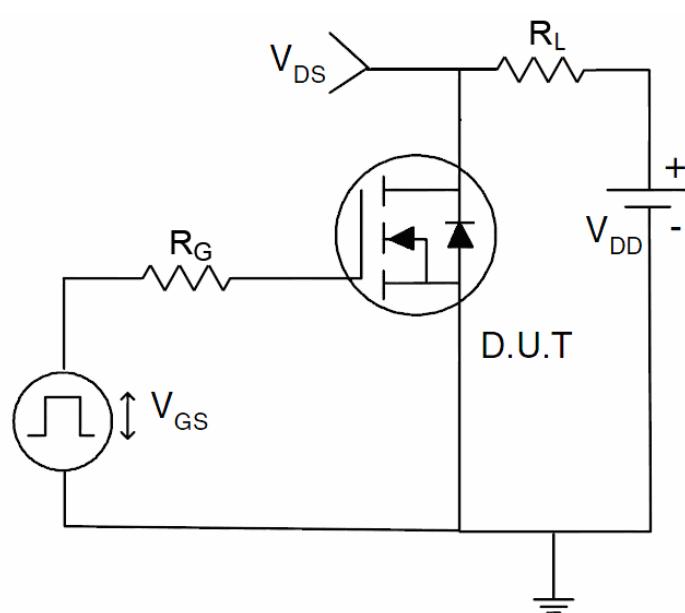
1) AS Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

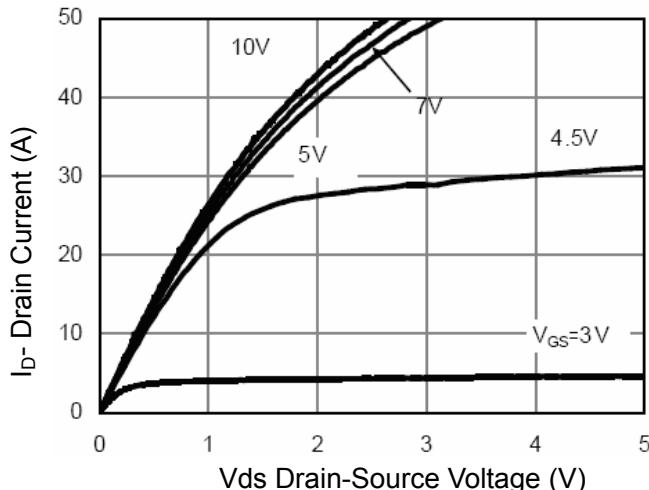


Figure 1 Output Characteristics

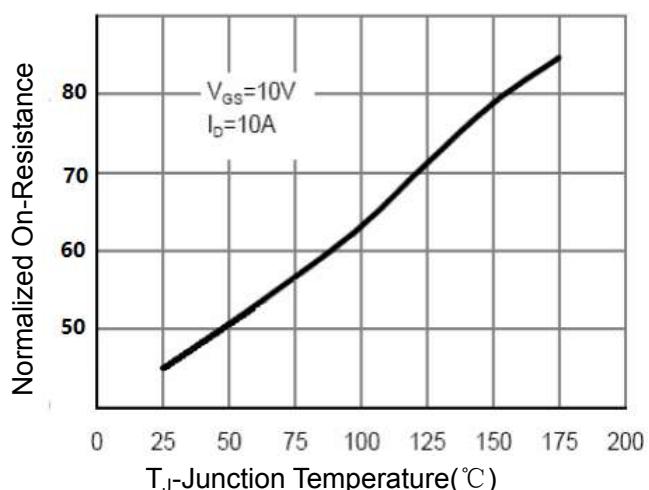


Figure 4 Rdson-JunctionTemperature

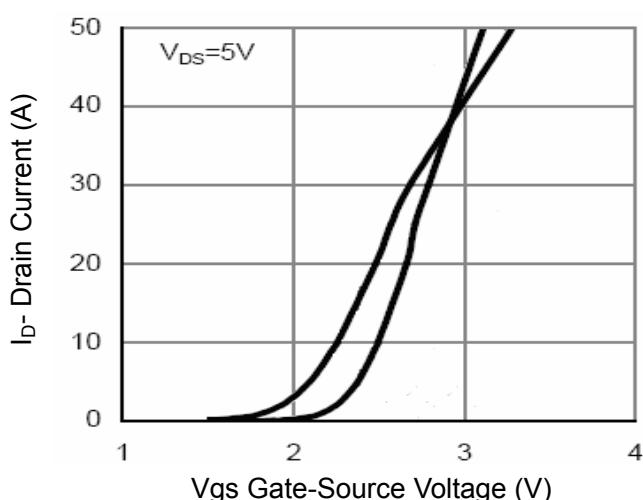


Figure 2 Transfer Characteristics

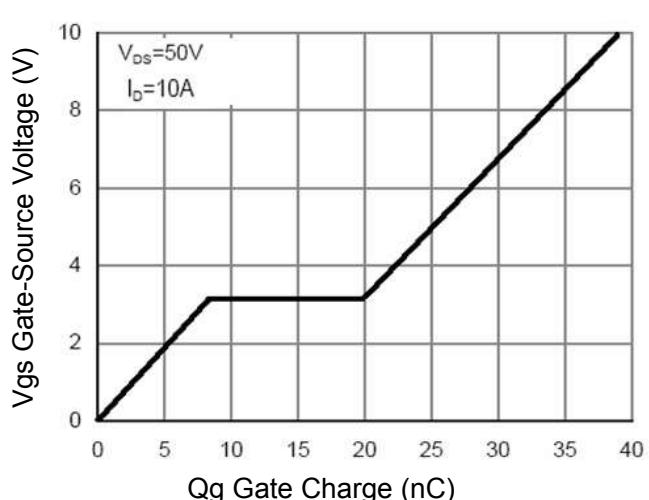


Figure 5 Gate Charge

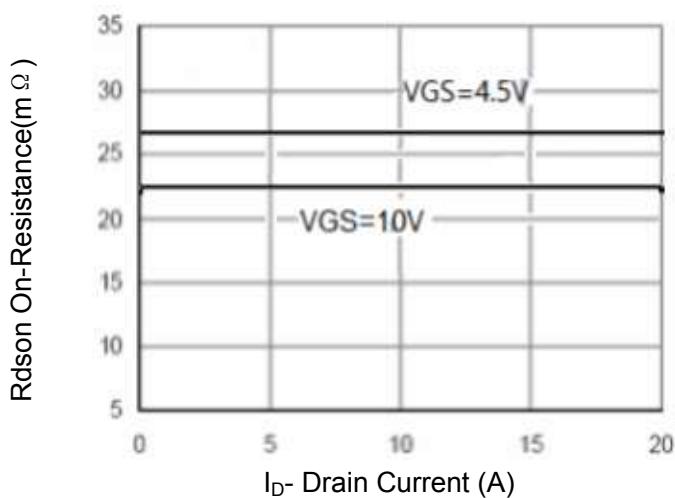


Figure 3 Rdson- Drain Current

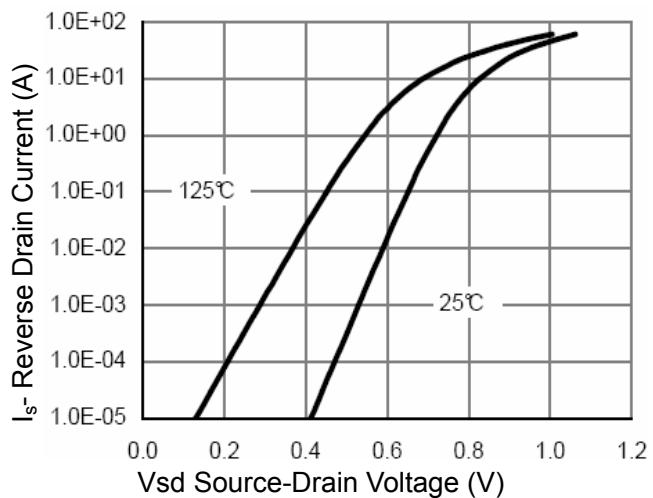


Figure 6 Source- Drain Diode Forward

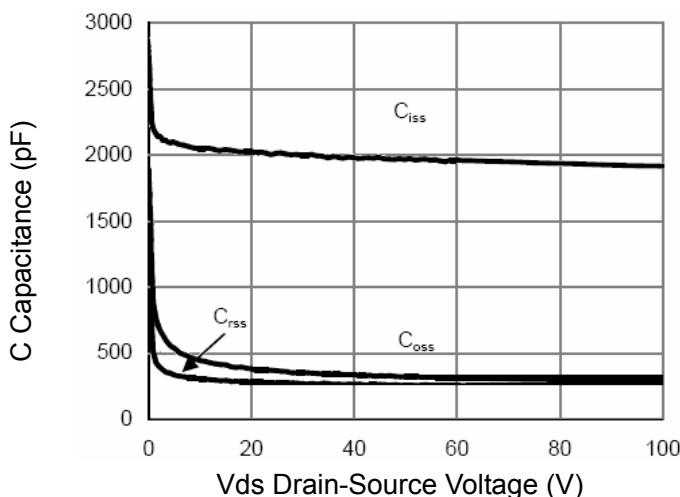
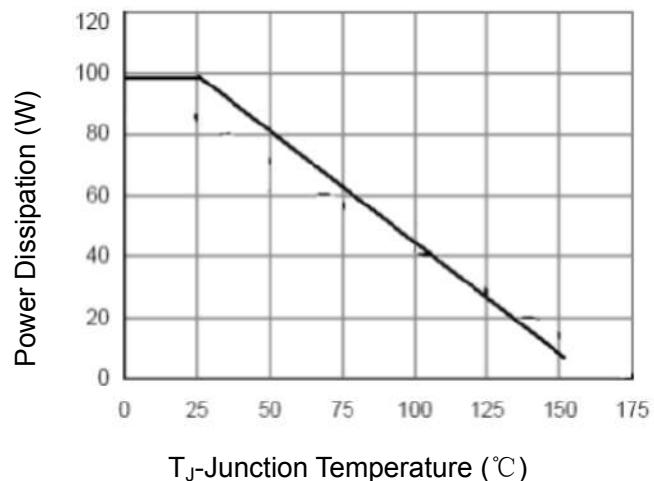


Figure 7 Capacitance vs Vds



T_j-Junction Temperature (°C)

Figure 9 Power De-rating

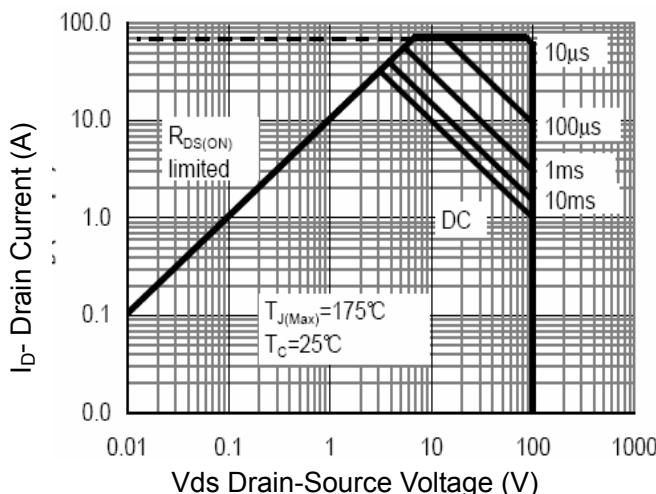
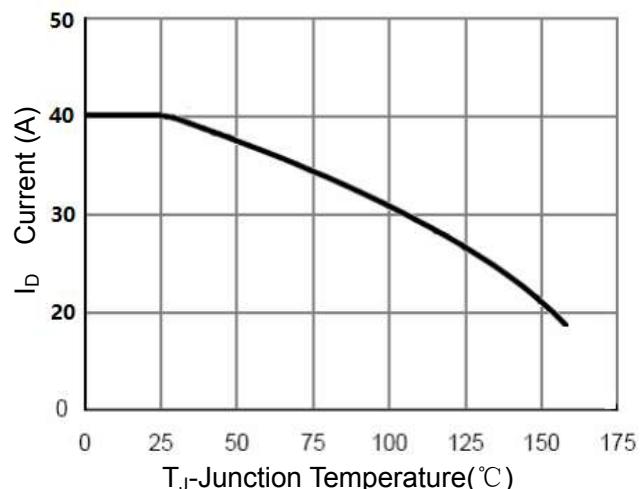
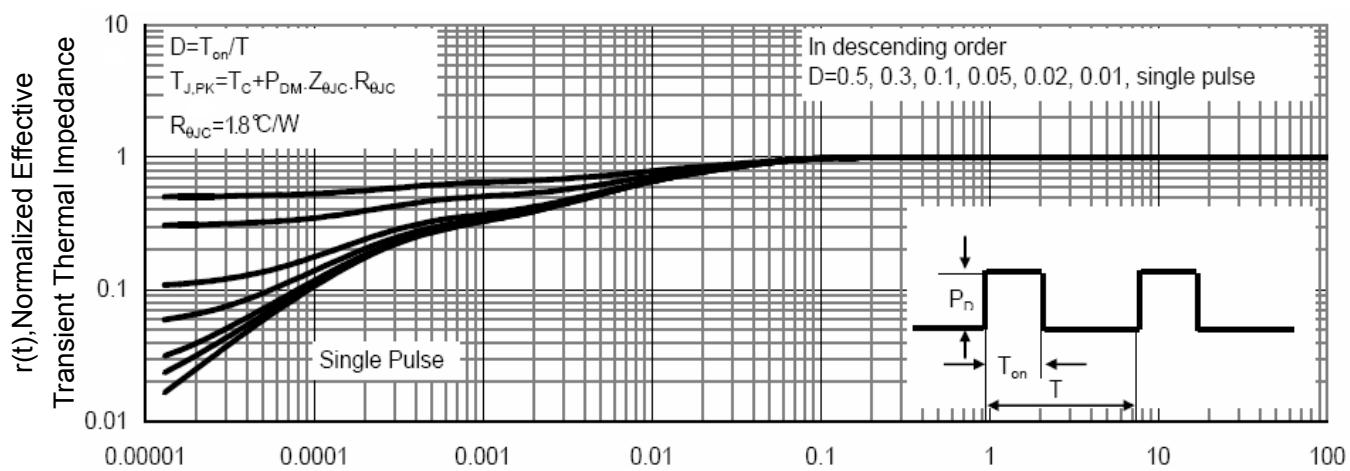


Figure 8 Safe Operation Area



T_j-Junction Temperature(°C)

Figure 10ID Current- Junction Temperature

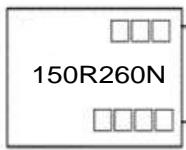


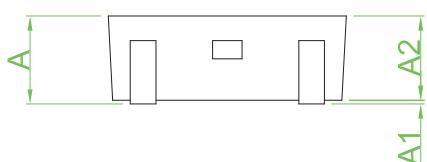
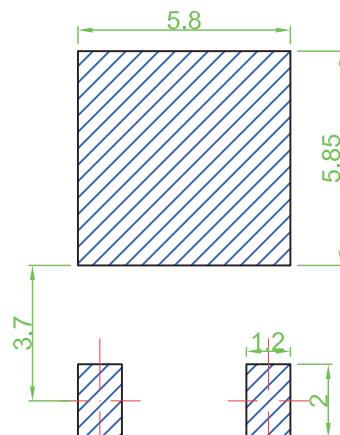
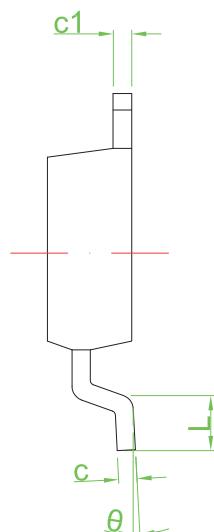
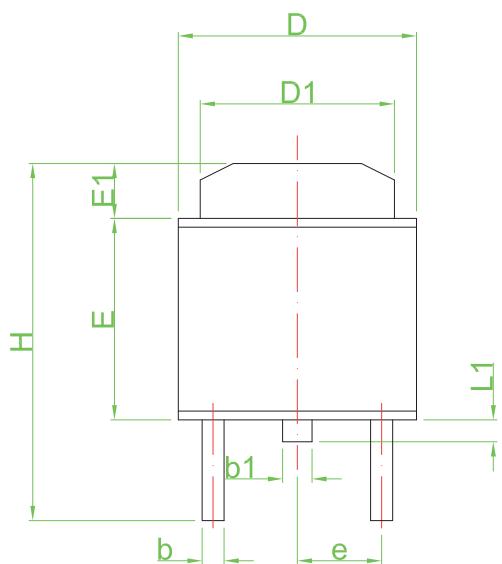
Square Wave Pulse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

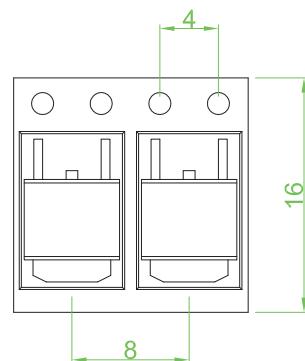
Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
JMD150R260NKQ-R	150R260N	TO-252	Tape& Reel	2500/Reel

PACKAGE	MARKING
TO-252	 <p>The marking diagram shows a rectangular label with the text "150R260N" in the center. Above the text are three small squares representing a lot number, and below the text are four small squares representing a date code. Arrows point from these square groups to the labels "Lot Number" and "Date Code" respectively.</p>



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.25	2.65	0.089	0.104
A1	0.00	0.15	0.000	0.006
A2	2.20	2.40	0.087	0.094
b	0.50	0.70	0.020	0.028
b1	0.70	0.90	0.028	0.035
c	0.46	0.66	0.018	0.026
c1	0.46	0.66	0.018	0.026
D	6.30	6.70	0.248	0.264
D1	5.20	5.40	0.205	0.213
E	5.30	5.70	0.209	0.224
E1	1.40	1.60	0.055	0.063
H	9.40	9.90	0.370	0.390
e	2.30 TYP		0.09 TYP	
L	1.40	1.77	0.055	0.070
L1	0.50	0.70	0.020	0.028
θ	0°	8°	0°	8°



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