

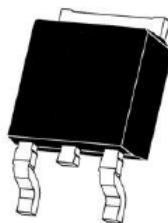
Features

- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5$ V
- Fast Switching
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

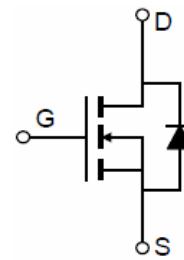
Product Summary



V_{DS}	30	V
$R_{DS(on),TYP}$ @ $V_{GS}=10$ V	2.5	$m\Omega$
I_D	120	A



TO-252-2L top view



Schematic diagram

Maximum ratings, at $T_A = 25^\circ C$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		30	V
I_S	Diode continuous forward current	$T_c = 25^\circ C$	120	A
I_D	Continuous drain current@ $V_{GS}=10V$	$T_c = 25^\circ C$	120	A
		$T_c = 100^\circ C$	80	A
I_{DM}	Pulse drain current tested ①	$T_c = 25^\circ C$	480	A
EAS	Avalanche energy, single pulsed ②		100	mJ
P_D	Maximum power dissipation	$T_c = 25^\circ C$	45	W
V_{GS}	Gate-Source voltage		± 20	V
$T_{STG} T_J$	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	62	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_j=85^\circ\text{C}$)	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	--	--	30	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
$V_{\text{GS}(\text{TH})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^③	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=30\text{A}$	--	2.5	3.5	$\text{m}\Omega$
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^③	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=30\text{A}$	--	3.9	4.5	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	--	2921	--	pF
C_{oss}	Output Capacitance		--	440	--	pF
C_{rss}	Reverse Transfer Capacitance		--	416	--	pF
R_g	Gate Resistance	f=1MHz	--	1.2	--	Ω
Q_g	Total Gate Charge	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=10\text{V}$	--	63	--	nC
Q_{gs}	Gate-Source Charge		--	13	--	nC
Q_{gd}	Gate-Drain Charge		--	16	--	nC
Switching Characteristics						
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DD}}=20\text{V}, I_{\text{D}}=20\text{A}, R_{\text{G}}=3\Omega, V_{\text{GS}}=10\text{V}$	--	14	--	nS
t_r	Turn-on Rise Time		--	18	--	nS
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		--	99	--	nS
t_f	Turn-Off Fall Time		--	45	--	nS
Source- Drain Diode Characteristics@ $T_j = 25^\circ\text{C}$ (unless otherwise stated)						
V_{SD}	Forward on voltage	$I_{\text{SD}}=20\text{A}, V_{\text{GS}}=0\text{V}$	--	0.79	1.2	V
t_{rr}	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_{\text{sd}}=20\text{A}, V_{\text{GS}}=0\text{V}$ $dI/dt=100\text{A}/\mu\text{s}$	--	32	--	nS
Q_{rr}	Reverse Recovery Charge		--	31	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by $T_{j\text{max}}$, starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_g = 25\Omega$, $I_{AS} = 20\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

Typical Characteristics

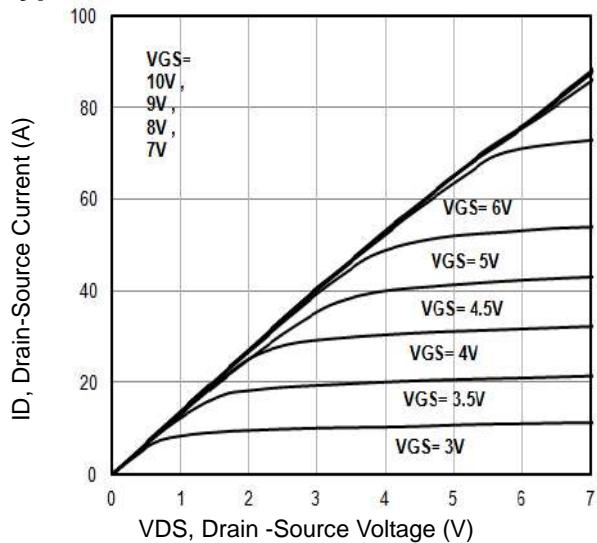


Fig1. Typical Output Characteristics

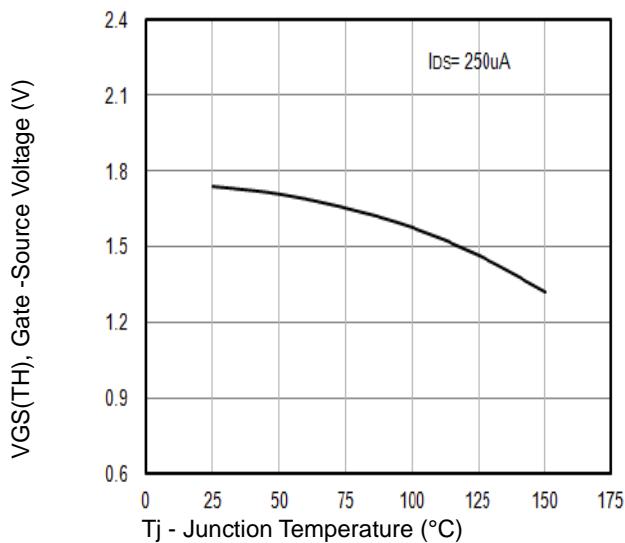


Fig2. $V_{GS(TH)}$ Gate-Source Threshold Voltage (T_j) (°C)

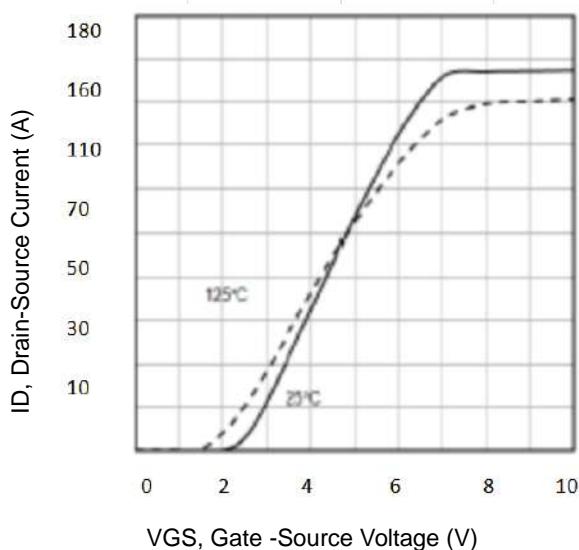


Fig3. Typical Transfer Characteristics

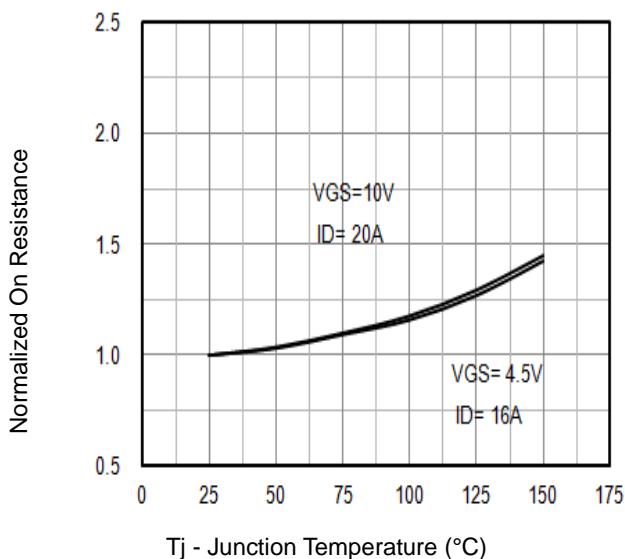


Fig4. Normalized On-Resistance Vs. T_j

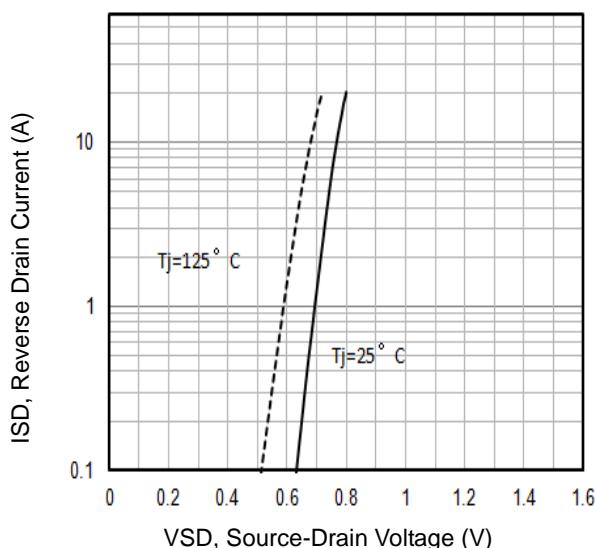


Fig5. Typical Source-Drain Diode Forward Voltage

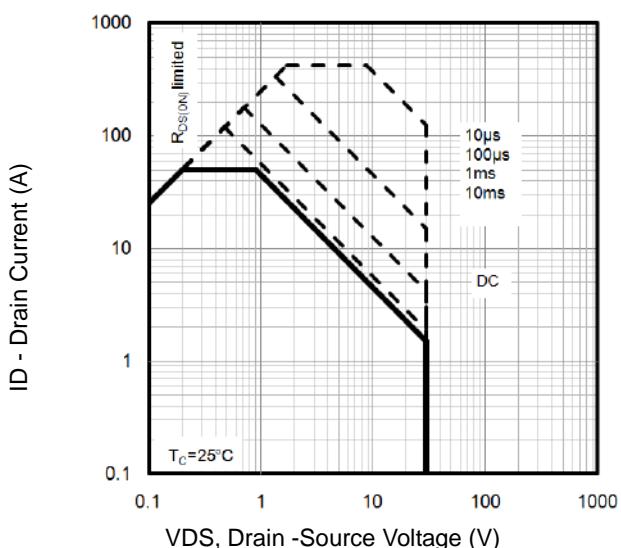


Fig6. Maximum Safe Operating Area

Typical Characteristics

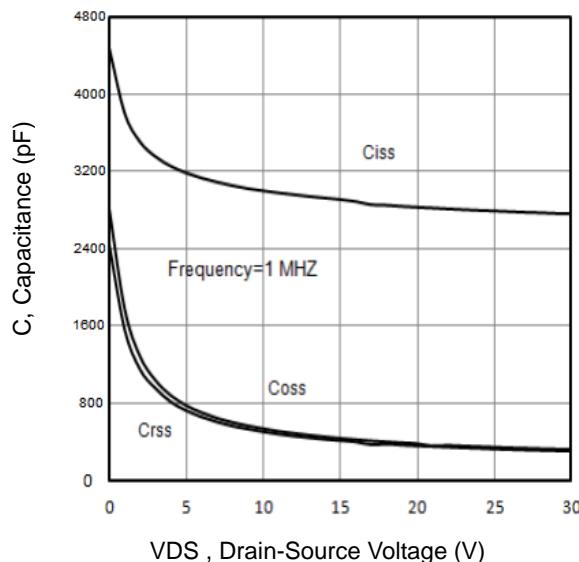


Fig7. Typical Capacitance Vs.Drain-Source Voltage

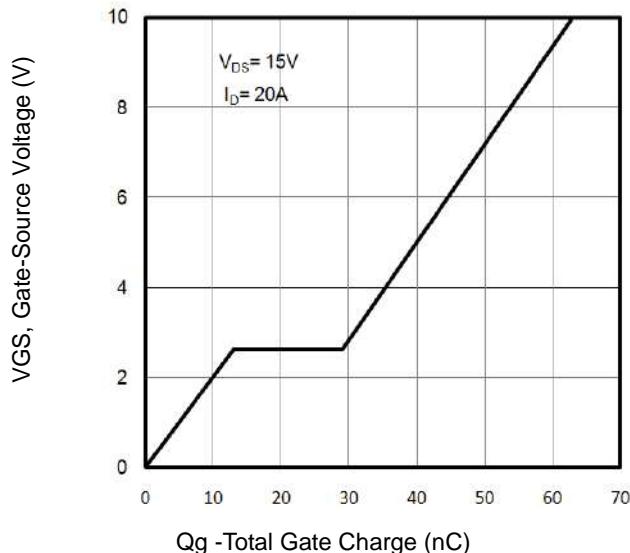


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

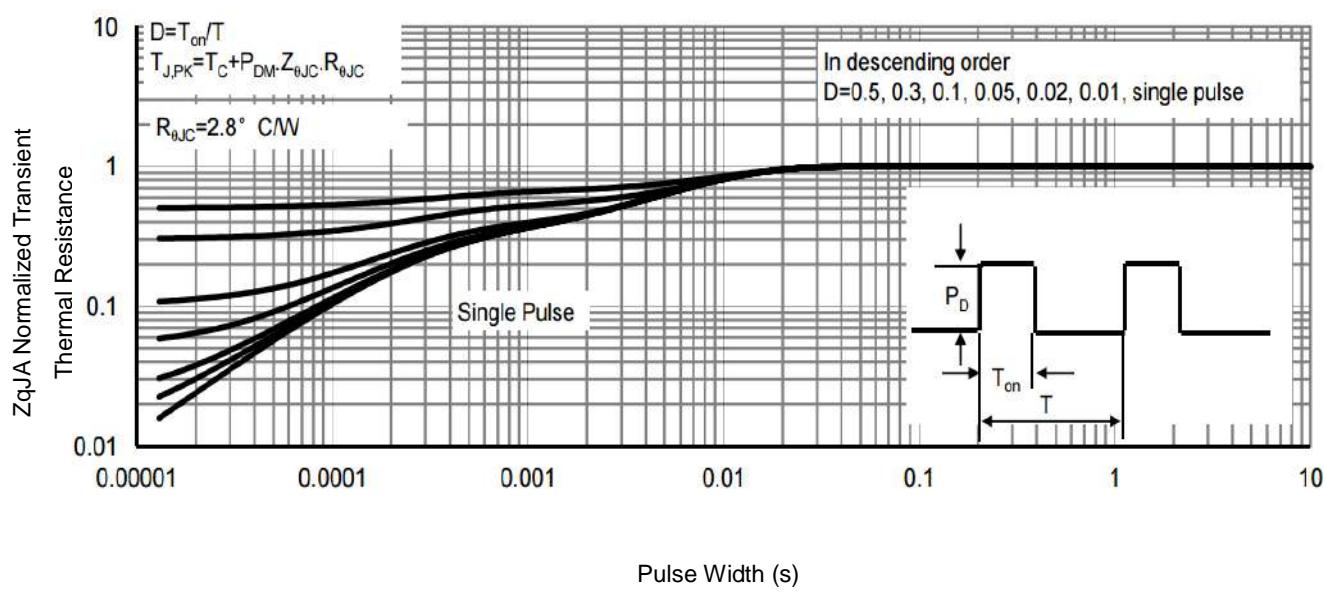


Fig9. Normalized Maximum Transient Thermal Impedance

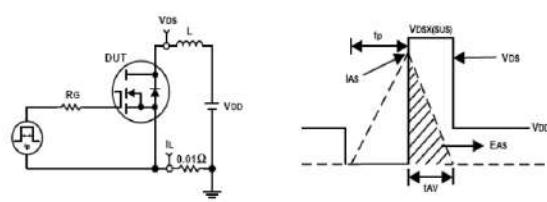


Fig10. Unclamped Inductive Test Circuit and waveforms

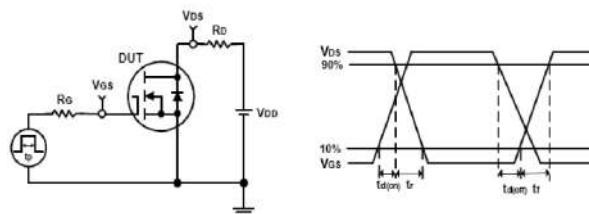
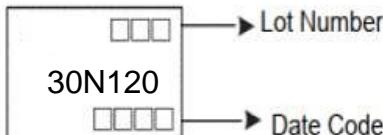


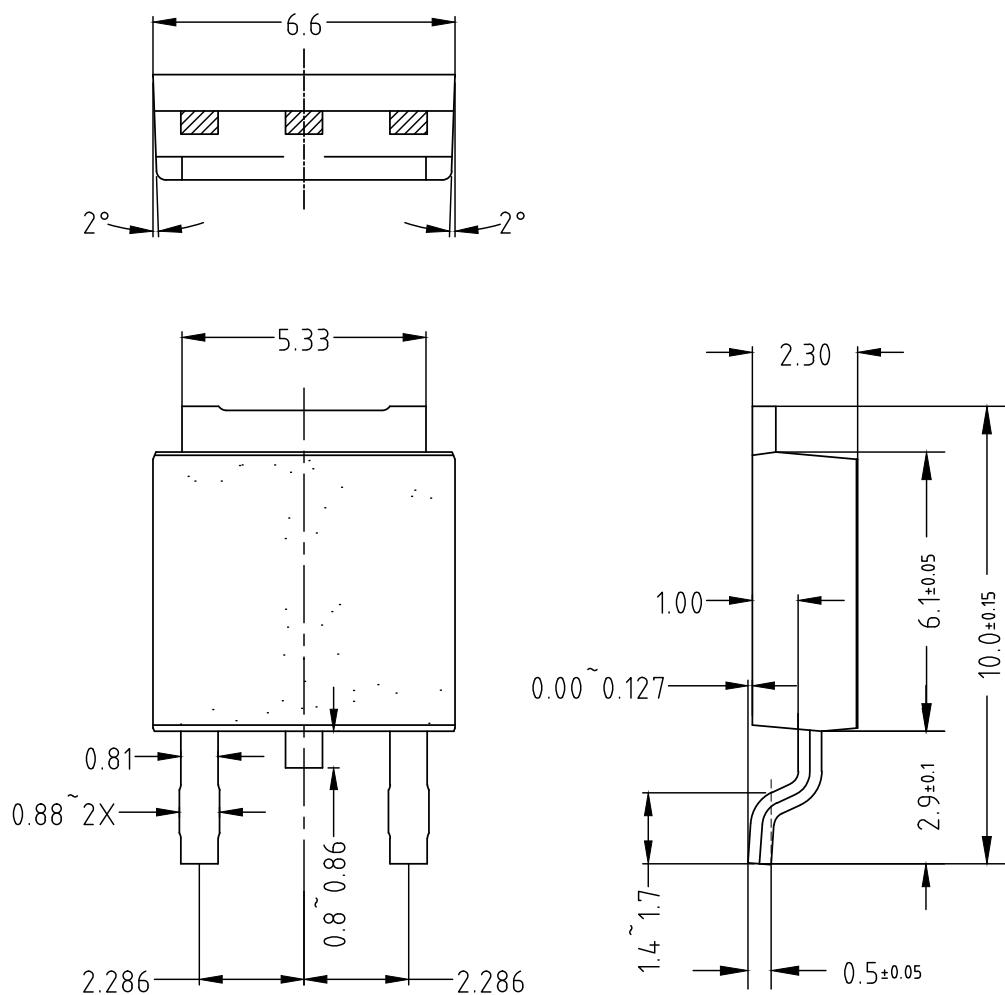
Fig11. Switching Time Test Circuit and waveforms

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
JMD30N120KQ-R	30N120	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 <p>The marking diagram illustrates the layout for a TO-252 package. The marking consists of three rows of characters and symbols. The top row contains three small squares, with an arrow pointing to the right labeled "Lot Number". The middle row contains the text "30N120". The bottom row contains four small squares, with an arrow pointing to the right labeled "Date Code".</p>

TO-252



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