

### General Features

- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

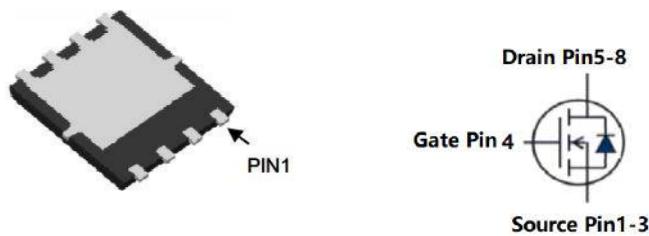
### Product Summary



$V_{DS}$	100	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	3.7	$\text{m}\Omega$
$I_D$	90	A

### Application

- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply



**DFN5x6-8L**

### Absolute Maximum Ratings ( $T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Condition	Value	Unit
$V_{DS}$	Drain-Source Voltage		100	V
$I_D$	Continuous Drain Current <sup>1</sup>	$T_c=25^\circ\text{C}$	90	A
		$T_c=70^\circ\text{C}$	48	A
$V_{GS}$	Gate-Source Voltage		$\pm 20$	V
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	$T_c=25^\circ\text{C}$	360	A
$P_D$	Total Power Dissipation	$T_c=25^\circ\text{C}$	60	W
$T_{STG}$	Storage Temperature Range		-55 to 150	°C
$T_J$	Operating Junction Temperature		-55 to 150	°C

## Thermal Data

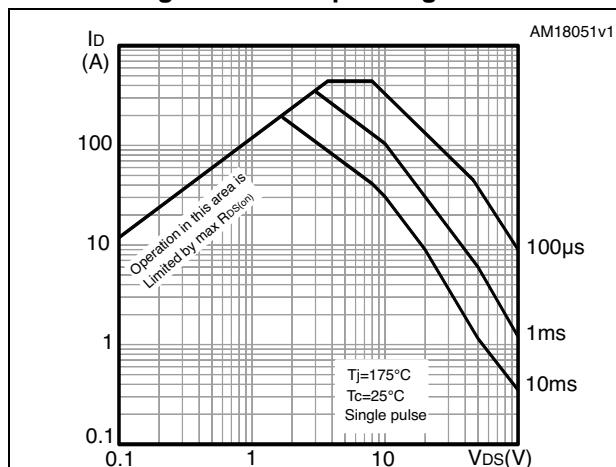
Symbol	Parameter	Typ.	Max	Unit
$R_{0JA}$	Thermal Resistance-Junction to Ambient	--	63	°C/W
$R_{0JC}$	Thermal Resistance-Junction to Case	--	1.3	

## Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise specified)

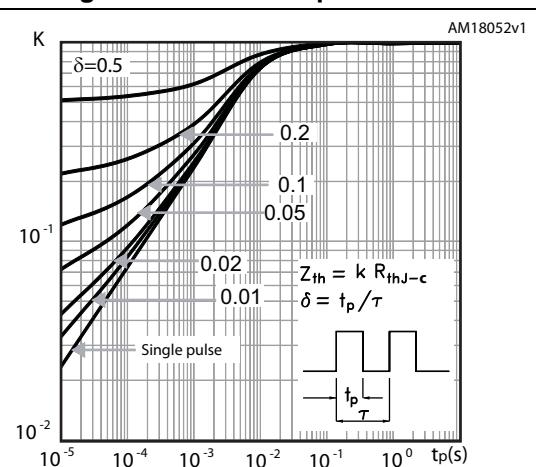
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>Static Characteristic</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$	100	--	--	V
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_D=250\mu\text{A}$	2	3.0	4	V
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=80\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	uA
		$V_{\text{DS}}=48\text{V}, V_{\text{GS}}=0\text{V}$	--	--	100	
$I_{\text{GSS}}$	Gate -Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	$\pm 100$	nA -
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=10\text{V}, I_D=20\text{A}$	-	3.7	4.5	mΩ
<b>Dynamic Characteristic</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}}=40\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	--	2890	--	pF
$C_{\text{oss}}$	Output Capacitance		--	881	--	
$C_{\text{rss}}$	Reverse Transfer Capacitance		--	13.2	--	
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=40\text{V}, V_{\text{GS}}=10\text{V}, R_G=2\Omega, I_D=20\text{A}$	--	16	--	nS
$t_r$	Turn-On Rise Time		--	13	--	
$t_{\text{d(off)}}$	Turn-off Delay Time		--	28	--	
$t_f$	Turn-Off Fall Time		--	7.5	--	
<b>Gate Charge Characteristic</b>						
$Q_g$	Total Gate Charge	$V_{\text{DD}}=30\text{V}, V_{\text{GS}}=10\text{V}, I_D=30\text{A}$	--	23	--	nC
$Q_{\text{gs}}$	Gate-Source Charge		--	5.2	--	
$Q_{\text{gd}}$	Gate-Drain Charge		--	7.3	--	
<b>Reverse diode Characteristic</b>						
$V_{\text{SD}}$	forward on voltage	$I_{\text{SD}}=20\text{A}, V_{\text{GS}}=0\text{V}$	--	--	1.2	V
$t_{\text{rr}}$	Reverse Recovery Time	$V_R=0\text{V}, I_F=20\text{A}, DI_F/dt=100\text{A/uS}$	--	46	--	nS
$Q_{\text{rr}}$	Reverse Recovery Charge		--	182	--	nC

### Typical Electrical and Thermal Characteristics (Curves)

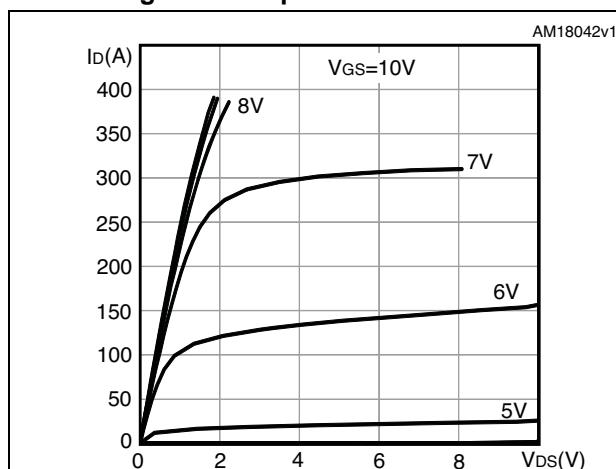
**Figure 2. Safe operating area**



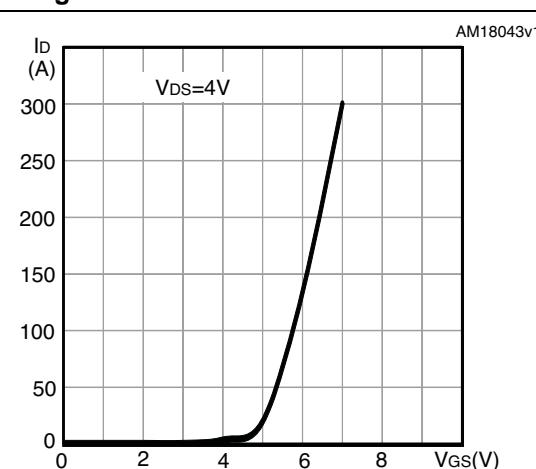
**Figure 3. Thermal impedance**



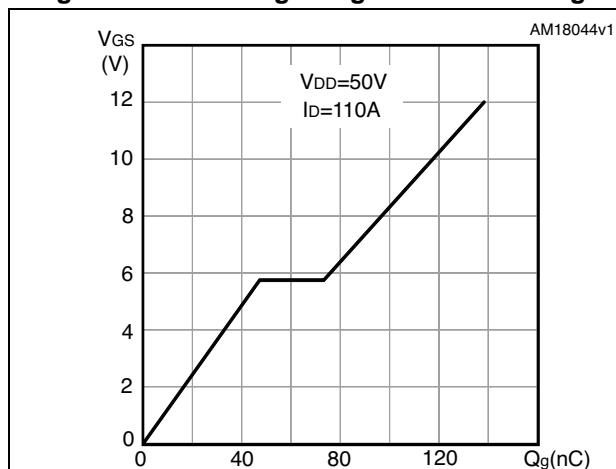
**Figure 4. Output characteristics**



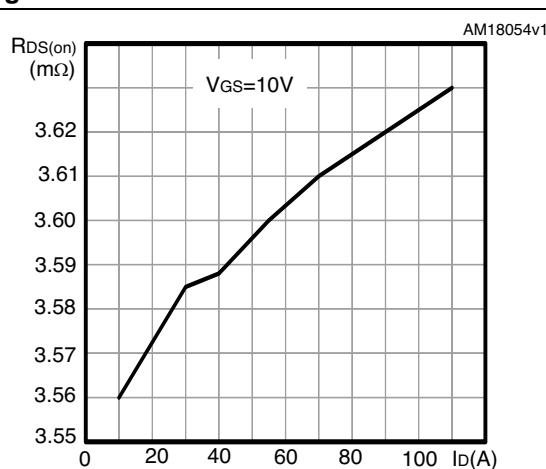
**Figure 5. Transfer characteristics**



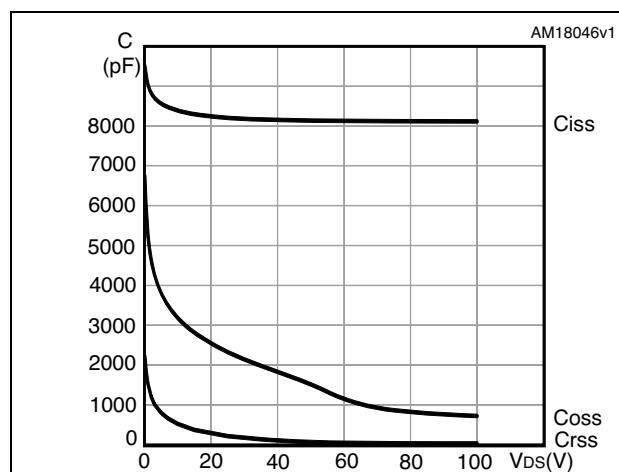
**Figure 6. Gate charge vs gate-source voltage**



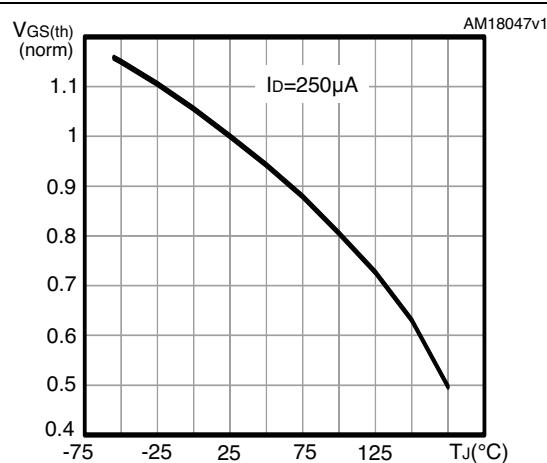
**Figure 7. Static drain-source on-resistance**



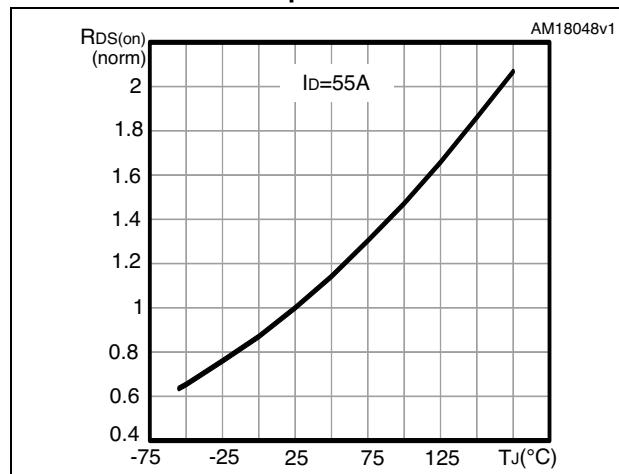
**Figure 8. Capacitance variations**



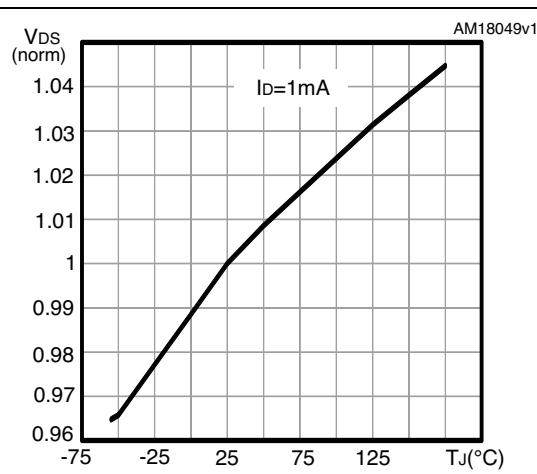
**Figure 9. Normalized gate threshold voltage vs temperature**



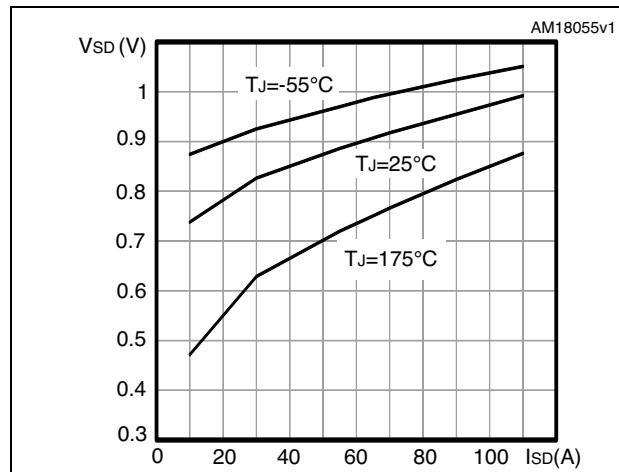
**Figure 10. Normalized on-resistance vs temperature**



**Figure 11. Normalized  $V_{DS}$  vs temperature**

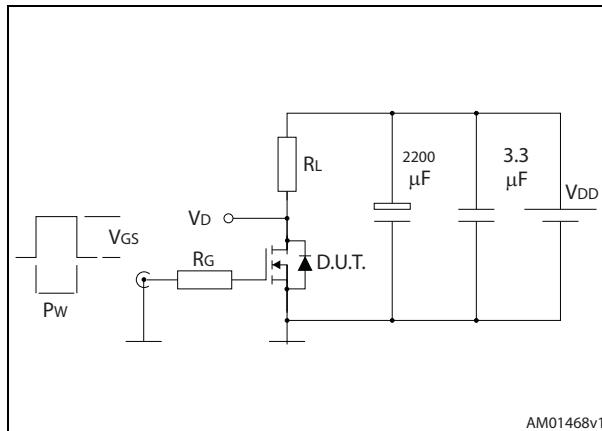


**Figure 12. Source-drain diode forward characteristics**

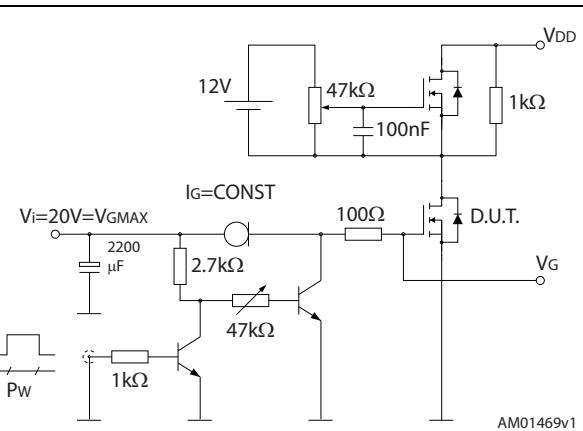


## Test circuits

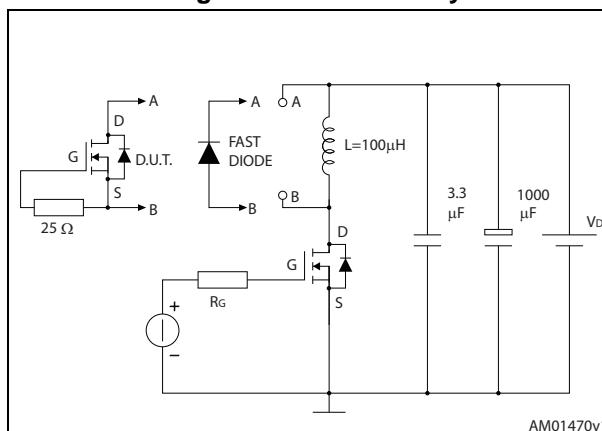
**Figure 13. Switching times test circuit for resistive load**



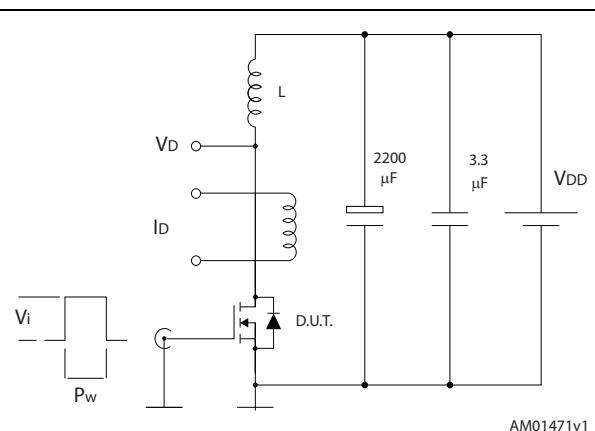
**Figure 14. Gate charge test circuit**



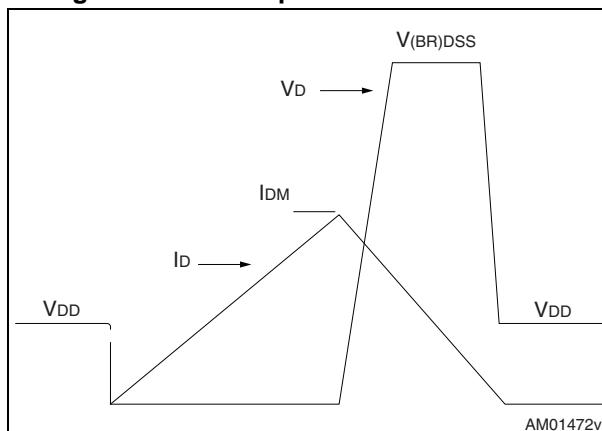
**Figure 15. Test circuit for inductive load switching and diode recovery times**



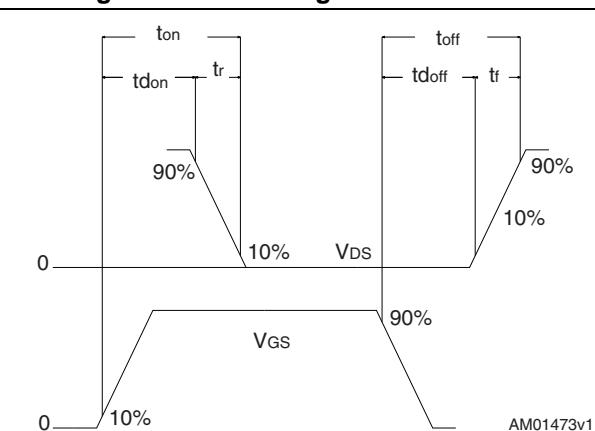
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**

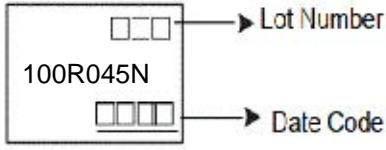


**Figure 18. Switching time waveform**

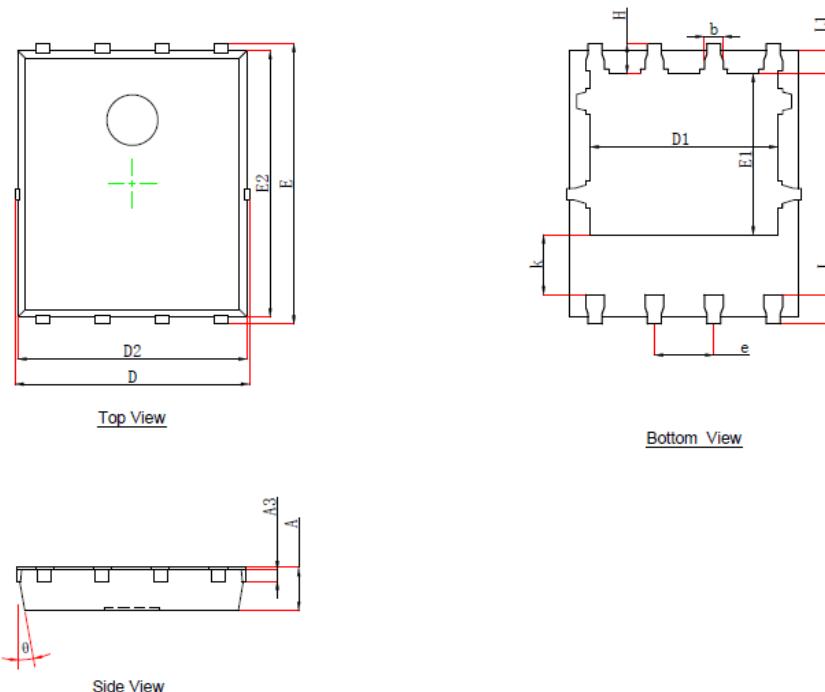


## Ordering and Marking Information

Ordering Device No	Marking	Package	Packing	Quantity
JMN100R045NQ-R	100R045N	DFN5*6-8	Tape&Reel	4000

PACKAGE	MARKING
DFN5*6-8	 <p>The marking diagram shows a rectangular box divided into three horizontal sections. The top section contains two small squares labeled "Lot Number". The middle section contains the text "100R045N". The bottom section contains four small squares labeled "Date Code".</p>

**DFN5\*6, 8 Leads**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	10°	12°	10°	12°

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