

## Features

- High density cell design for ultra low R<sub>ds(on)</sub>
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

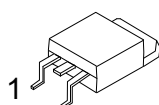
## Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

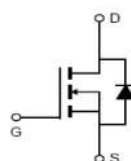
## Product Summary



$V_{DS}$	30	V
$R_{DS(on),TYP@ V_{GS}=10V}$	9	mΩ
$I_D$	50	A



TO-252



N-Channel MOSFET

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous	$I_D$	50	A
Drain Current-Continuous( $T_C=100^{\circ}C$ )	$I_D(100^{\circ}C)$	35	A
Pulsed Drain Current	$I_{DM}$	140	A
Maximum Power Dissipation	$P_D$	60	W
Derating factor		0.4	W/ $^{\circ}C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	70	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^{\circ}C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.5	$^{\circ}C/W$
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**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

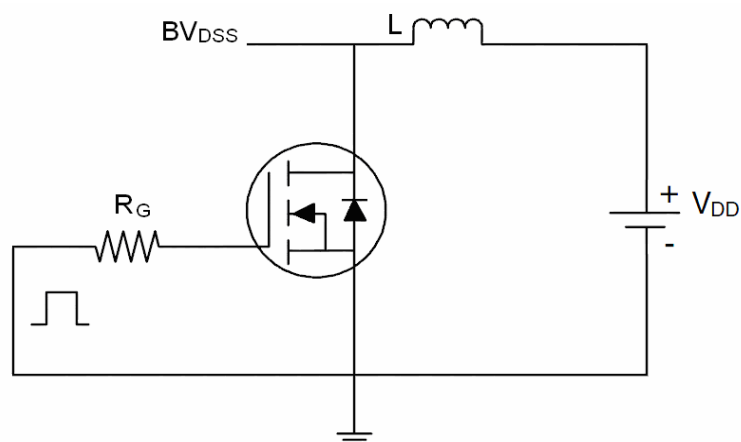
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.4	2	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =25A	-	9	11	mΩ
		V <sub>GS</sub> =5V, I <sub>D</sub> =20A	-	11.3	14	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	15	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C <sub>OSS</sub>		-	280	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	160	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =20A V <sub>GS</sub> =10V, R <sub>GEN</sub> =1.8Ω	-	10	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	8	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	30	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	5	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =25A, V <sub>GS</sub> =10V	-	23	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	7	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	4.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =25A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	50	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 50A di/dt = 100A/μs (Note 3)	-	22	35	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	11	18	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

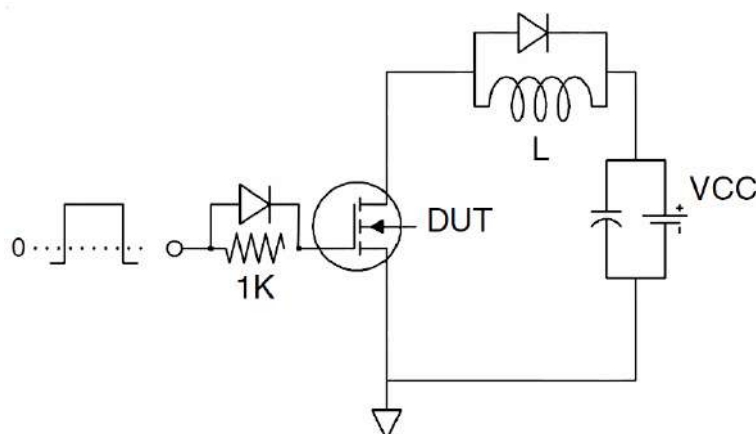
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=15V, V<sub>G</sub>=10V, L=1mH, R<sub>g</sub>=25Ω

## Test circuit

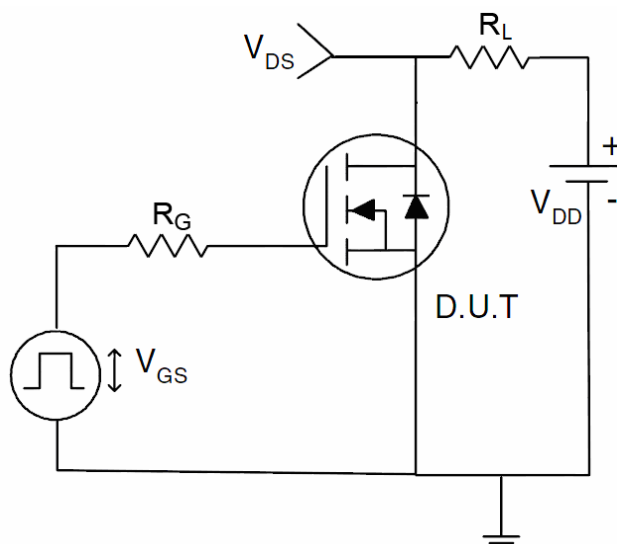
### 1) $E_{AS}$ test Circuits



### 2) Gate charge test Circuit:



### 3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

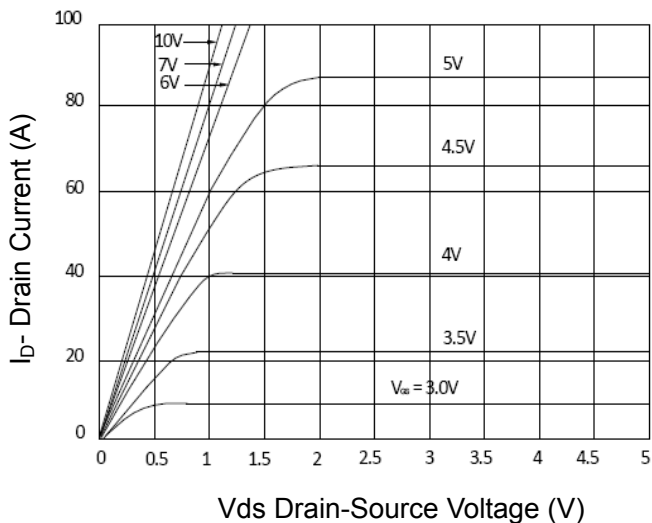


Figure 1 Output Characteristics

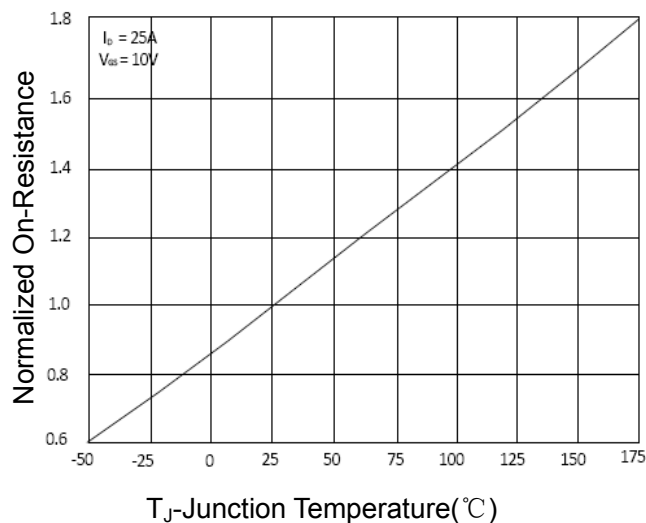


Figure 4  $R_{dson}$ -Junction Temperature

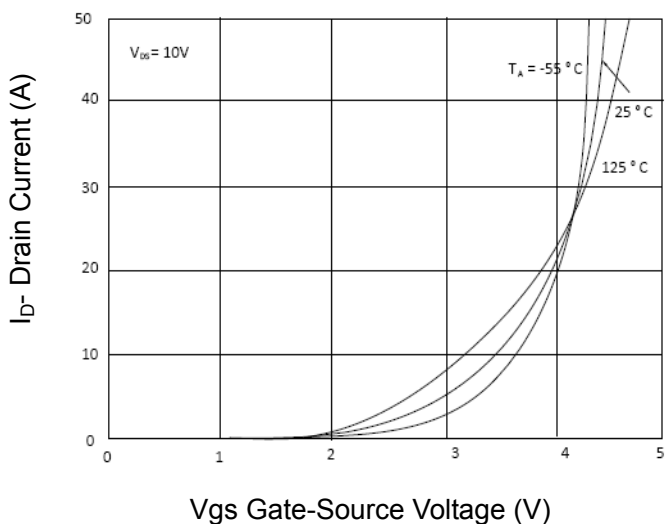


Figure 2 Transfer Characteristics

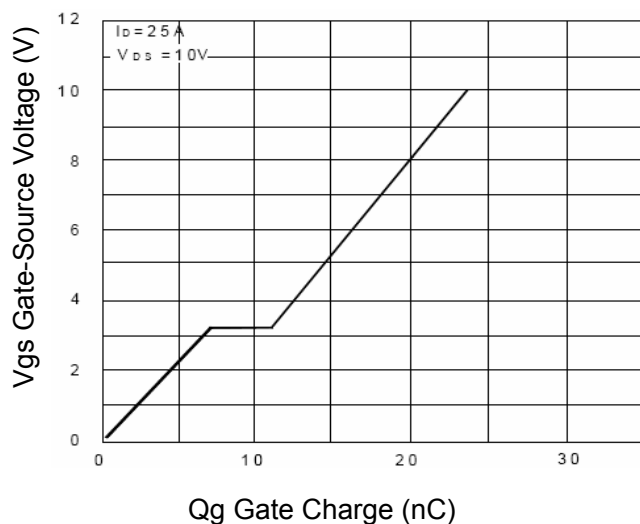


Figure 5 Gate Charge

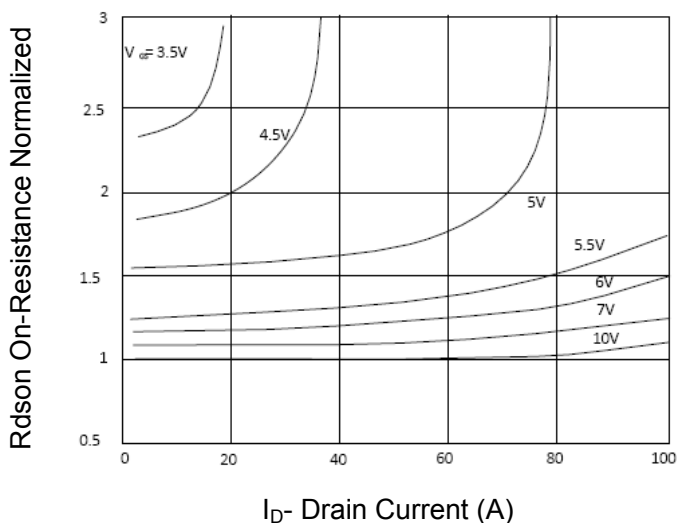


Figure 3  $R_{dson}$ - Drain Current

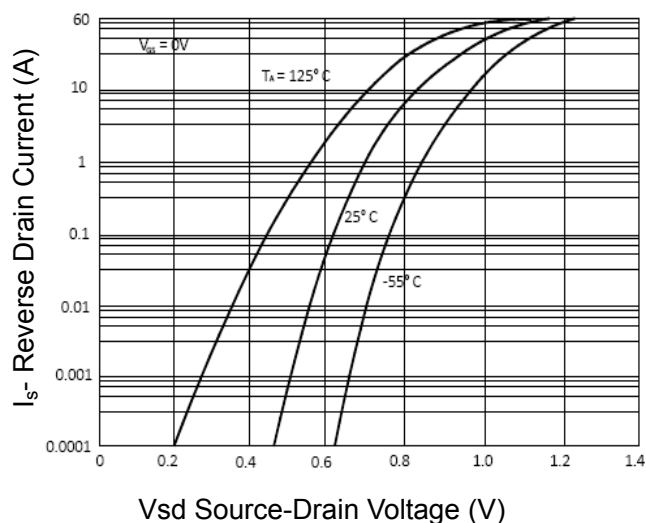


Figure 6 Source- Drain Diode Forward

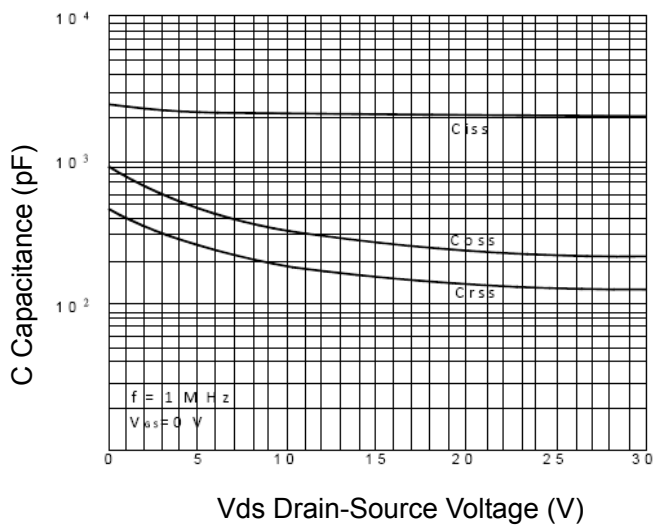


Figure 7 Capacitance vs Vds

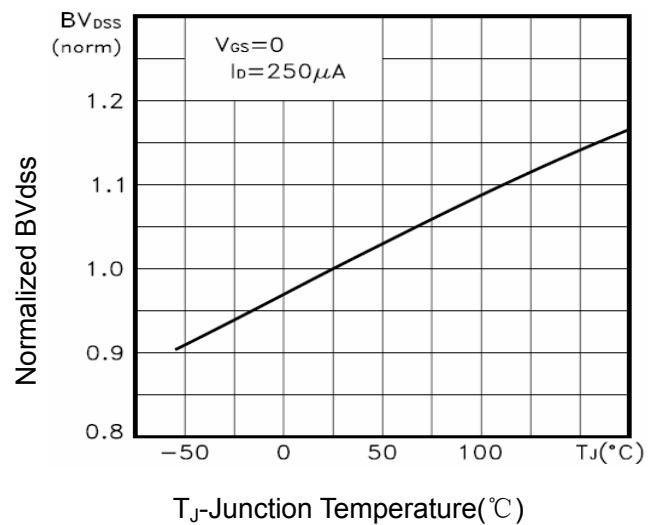


Figure 9  $BV_{DSS}$  vs Junction Temperature

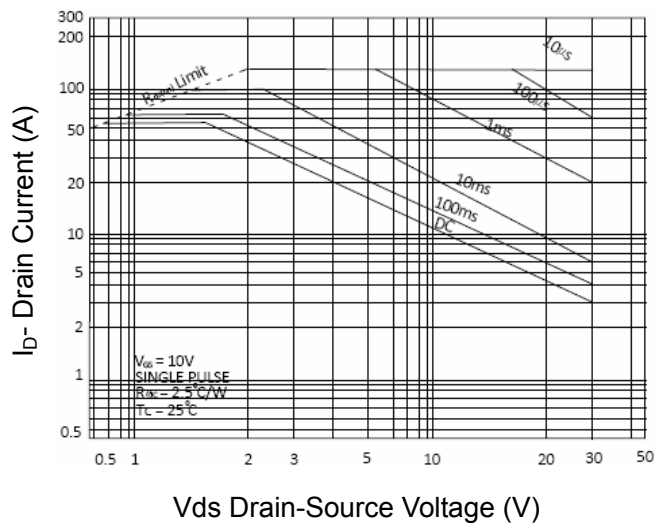


Figure 8 Safe Operation Area

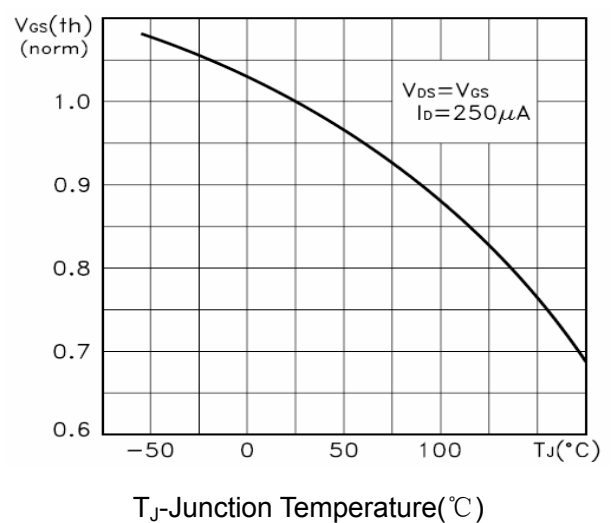


Figure 10  $V_{GS(th)}$  vs Junction Temperature

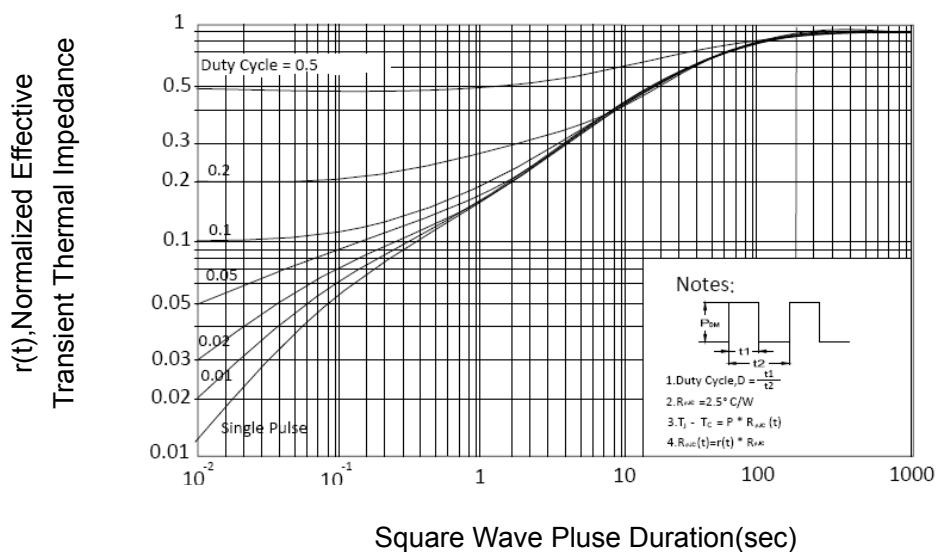
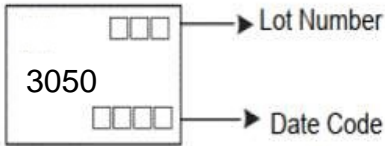
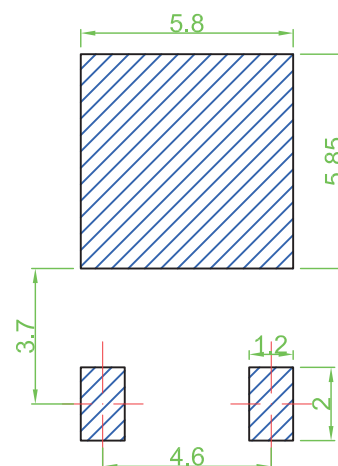
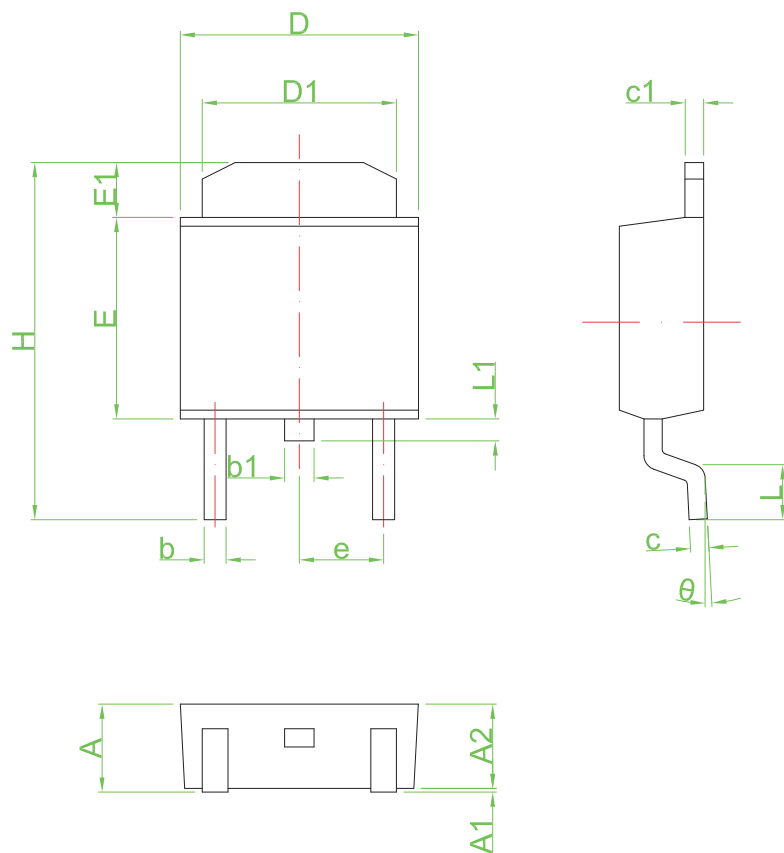


Figure 11 Normalized Maximum Transient Thermal Impedance

## Ordering and Marking Information

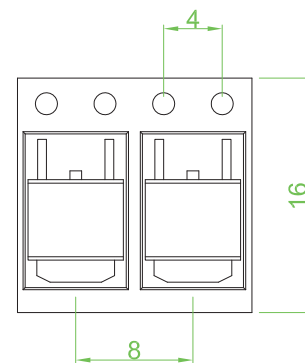
Ordering Device No.	Marking	Package	Packing	Quantity
JMD3050KQ-R	3050	TO-252	Tape&Reel	2500

PACKAGE	MARKING
TO-252	 <p>The diagram shows a rectangular marking area. In the center is the number '3050'. Above it are two small squares representing the Lot Number. Below it are four small squares representing the Date Code. Arrows point from the text 'Lot Number' and 'Date Code' to their respective boxes.</p>



Recommended Land Pattern

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.25	2.65	0.089	0.104
A1	0.00	0.15	0.000	0.006
A2	2.20	2.40	0.087	0.094
b	0.50	0.70	0.020	0.028
b1	0.70	0.90	0.028	0.035
c	0.46	0.66	0.018	0.026
c1	0.46	0.66	0.018	0.026
D	6.30	6.70	0.248	0.264
D1	5.20	5.40	0.205	0.213
E	5.30	5.70	0.209	0.224
E1	1.40	1.60	0.055	0.063
H	9.40	9.90	0.370	0.390
e	2.30 TYP		0.09 TYP	
L	1.40	1.77	0.055	0.070
L1	0.50	0.70	0.020	0.028
theta	0°	8°	0°	8°



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